R & T PROJECT CODE=> 414f004---09 PREV R & T PROJECT CODE=> 414f004---08
PR SUBMISSION DATE-> 12 DEC 1990
CONTRACTOR NAME=> Purdue Research Foundation
PR TYPE CODE=> if
SO CODE=> 414SS
ITC=> grt
STARS PR NO=> ~~N0001491PR24h97~~ was committed under N000 14 91 PR24595 (b) (6)

FRC	PROGRAM YEAR	FUNDS INCREMENT	FUNDS EXPIRATION DATE	FS
4145	1991	97500.00	30 SEP 1991	a

Notes to 500:
No Text Available.

Notes to 600:
This provides the final funding increment to the contract.

Accounting Classification

ACRN-FRC-PY-----APPN------SUBHD-OBJ-BCN-SA--AAA---TT--PAA----COST CODE-----PE--
AC 4145 1991 1711319 .W1AE 000 RA414 0 068342 2B 000000 021020000100 0601153N
Funds Source Title: ONR1RDN
Source for initialization: RPDP-5-91 CODE 111

Short Work Statement:
Investigate materials, techniques, designs, and fabrication procedures leading to high speed memory circuits exhibiting apriori controlled threshold voltages having little deviation and extremely long refresh times.

Extended Work Statement:
Investigate MESFET and MODFET DRAM memories as per section IV (Statement of Work) of the proposal.

Stars (b) (6)
DBase 12.14.90 (b) (6)

R & T PROJECT CODE=> 414f004---09 PREV R & T PROJECT CODE=> 414f004---08
PR SUBMISSION DATE=> 12 DEC 1990
CONTRACT NUMBER=> N0001489J1864 CONTRACT MOD NUMBER-> P00002
START DATE OF CURRENT CONTRACT=> 01 FEB 1989 END DATE=> 31 DEC 1991
REQUESTED START DATE=> 01 NOV 1990 END DATE=> 31 DEC 1991
NEGOTIATED START DATE=> 01 ~~NOV 1990~~ JAN 1991
CONTRACTOR NAME=> Purdue Research Foundation
SHORT CONTRACTOR CODE-> purd SIZE AND TYPE BUSINESS CODE-> ls
CONTRACTOR STREET=> Hovde Hall, Third Floor
CONTRACTOR CITY=> West Lafayette
CONTRACTOR STATE=> IN CONTRACTOR ZIP CODE=> 47907
REP=> Chandrea Lightfoot PH=> 317 494 1077
PR TYPE CODE(1)=> if INSTRUMENT TYPE CODE=> grt
(2)=> BASIS FOR SELECTION=> baa
(3)=> EQUIPMENT TITLE=>

BRANCH HEAD APPROVAL OF SOURCE JUST./RFP=>y J E DATE=>27 AUG 1990
BRANCH HEAD COMMENTS ON SOURCE JUSTIFICATIONS=>

SECTION LEADER USERID=>kurzius SECTION LEADER CODE=>614--
SECTION LEADER NAME=>Kurzius ,Mark ,J .
DATE SECTION LEADER ASSIGNED=>27 AUG 1990 ASSIGN WEIGHT=>

NEGOTIATOR USERID=>~~gallman~~ Hudson NEGOTIATOR CODE=>614--
NEGOTIATOR NAME=>Gallmon ,Julia ,M .
DATE NEGOTIATOR ASSIGNED=>27 AUG 1990 1/15/91
PREVIOUS NEGOTIATOR NAME=> , , .
PCO USERID=>kurzius NAME=>Mark Kurzius CODE=>1513
S.O. NAME=>Yoder ,Max ,N .
S.O. USERID=>yoder S.O. CODE=>1114SS

TOTAL CUMULATIVE VALUE OF CURRENT CONTRACT=> 305000.00
TOTAL OBLIGATED FUNDING ON CURRENT CONTRACT=> 207500.00
PREV NEG INCREMENTAL FUNDS PROVIDED BY THIS PR=> ~~260000.00~~ 97500.00
NEW FUNDS BEING NEGOTIATED INTO CURRENT CONTRACT=> 0.00
CURRENTLY NEGOTIATED NEW FUNDS PROVIDED BY THIS PR=> 0.00
TOTAL EXPECTED TO BE OBLIGATED ON FUTURE ACTIONS=> 0.00

FRC	PROGRAM YEAR	FUNDS INCREMENT	FS	DUE DATE	ACRN	CSS FUNDS
4145	1991	97500.00	a	01 NOV 1990	AC	0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00

1498 TITLE=>(u)GaAs Gate Dynamic Memory Technology

REPORTS FREQUENCY CODE=>sem

PI NAME=>Michael R Melloch
PI TELEPHONE=>(317) 494 3528 EXT=>

CONTRACT PROPOSAL/REQUISTION NUMBER->

ONR PROPSOAL NUMBER=>

PATENTS INTEREST CODE=>

CLASSIFICATION DD 254=> DATE OF DD 254=>

Notes to 600:
This provides the final funding increment to the contract.

Short Work Statement:
Investigate materials, techniques, designs, and fabrication procedures leading to high speed memory circuits exhibiting apriori controlled threshold voltages having little deviation and extremely long refresh times.

Extended Work Statement:
Investigate MESFET and MODFET DRAM memories as per section IV (Statement of Work) of the proposal.

BPS:Submission,Eval,Cost/JA:Desc:

This proposal was received in response to the ONR announcement of research interest published in the COMMERCE BUSINESS DAILY of 28 APR 1988. Award is recommended based on evaluation of the proposal in accordance with the following criteria (BPS items 1-6):

Financial Considerations:

Labor -
The proposed quantities and types of labor (including any consultants and labor provided by subgrantee) are reasonable and necessary for accomplishing the research project.
The proposed labor rates are in line with standard academic or industrial practice for research of this type.
Any consulting at a rate in excess of $500.00 per day is justified in the "Additional Consultant Information" text item.

Other Direct Costs-
Other proposed direct costs (such as supplies, equipment, ADP, travel, etc.) are reasonable and necessary for accomplishing the research project.

I have reviewed and accepted the proposed budget subject to the

the principal investigator submit a revised budget through official university channels and that revised budget is enclosed. The proposal appears to be fair, reasonable, in the interest of the government, and is consistent with other previous and current efforts of this nature.

BPS:Overall Merits/JA:Contr Quals:
This work incorporates two novel ideas, synergistically combined. They are (a) a buried heterojunction charge storage well and (b) a semiconductor, zero interface state density FET gate separated by an undoped quantum barrier.

BPS:ONR Mission/JA:Enhance Comp:
If successful, this will result in the first GaAS dynamic Modfet random access memory. This should enable radiation hard memory technology operating at GHz clock speeds and with cell density 6 times that of present GaAs memories. Dense memories such as these will reduce interconnects among chips and improve military readiness and reliability.

BPS:Contr Quals/JA:Noncomp Justfctn:
The proposed contractor provides the unique capabilities and experience of the principal investigator as described in the research proposal. The principal investigator would not be available through any other contractor.

BPS:PI Quals/JA:Improve Comp:
The principal investigator is highly qualified to execute the proposed program based on his previous experience, publications, and presentations as described in the proposal.

1498 Technical Objective:
(U) This work seeks new low cost approaches to high speed memory required in future Navy signal processing systems.

1498 Approach:
(U) Buried heterojunction charge storage wells will be used in conjunction with semiconductor gates to create memory devices exhibiting very low (e.g., one hour) room temperature refresh times. MBE-grown aluminum arsenide and gallium arsenide will be used. Doped alloys will be avoided.

1498 Progress:
(U) Buried memory storage cells using the capacitance of a reversed biased P-N junction have been fabricated and tested. The cells include the associated storage cell transistor and the read and write transistors in the single cell memory "array". Storage times in excess of 0.5 minute at room temperature were achieved for the IC.

Accounting Classification

ACRN-FRC-PY-----APPN------SUBHD-OBJ-BCN-SA--AAA---TT--PAA----COST CODE-----PE--
AC 4145 1991 1711319 .W1AE 000 RA414 0 068342 2B 000000 021020000100 0601153
Funds Source Title: ONR1RDN
Source for Initialization: RPDP-5-91 CODE 111

Contractor Information:
Short Contractor Code: purd
Purdue Research Foundation
Division of Sponsored Programs
Hovde Hall, Third Floor
West Lafayette, IN 47907

Size & Type: 1s
Country: US
City Code: 82862
State Code: 18
Duns Code: 070710447
DLA Milscap Code: 48877
Payment Dodaad Code: N00179
ACO Milscap Code: N62880
Cognizant Audit Agency: hs05
TIN: 351052049
PTIN:

R & T PROJECT CODE=> 414f004---08 PREV R & T PROJECT CODE=> 414f004---07
PR SUBMISSION DATE=> 16 AUG 1990
CONTRACTOR NAME=> Purdue Research Foundation
PR TYPE CODE=> if
SO CODE=> 414SS
ITC=> grt
STARS PR NO=> N0001491PR24595

FRC	PROGRAM YEAR	FUNDS INCREMENT	FUNDS EXPIRATION DATE
4145	1991	130000.00	30 SEP 1991

FS
p 8/24/90

1498 TITLE=>(u)GaAs Gate Dynamic Memory Technology

Notes to 500:
No Text Available.

DO NOT EXECUTE
PR must be returned to Code 01122 for signatures prior to execution.
Released for execution by Code 01122 ..... date .....

Notes to 600:
This provides the final funding increment to the contract.

ccounting Classification

CRN-FRC-PY-----APPN------SUBHD-OBJ-BCN-SA--AAA---TT--PAA----COST CODE-----PE--
4145 1991 1711319 •WIAE 000 RA414 0 068342 2B 000000 021020000100 0601153N
unds Source Title: ONR1RDN
ource for Initialization: RPDP-5-91 CODE 111

ort Work Statement:
vestigate materials, techniques, designs, and fabrication procedures
ading to high speed memory circuits exhibiting apriori controlled
reshold voltages having little deviation and extremely long refresh
nes.

ended Work Statement:
estigate MESFET and MODFET DRAM memories as per section IV
atement of Work) of the proposal.

DBue 8.23.90 (b) (6)

R & T PROJECT CODE=> 414f004---08 PREV R & T PROJECT CODE=> 414f004---07
PR SUBMISSION DATE=> 16 AUG 1990
CONTRACT NUMBER=> N0001489J1864 CONTRACT MOD NUMBER=> P00001 2
START DATE OF CURRENT CONTRACT=> 01 FEB 1989 END DATE=> 31 DEC 1991
REQUESTED START DATE=> 01 NOV 1990 END DATE=> 31 DEC 1991
NEGOTIATED START DATE=> 01 NOV 1990

CONTRACTOR NAME=> Purdue Research Foundation
SHORT CONTRACTOR CODE=> purd SIZE AND TYPE BUSINESS CODE=> 1s
CONTRACTOR STREET=> Hovde Hall, Third Floor
CONTRACTOR CITY=> West Lafayette
CONTRACTOR STATE=> IN CONTRACTOR ZIP CODE=> 47907
REP=> Chandrea Lightfoot PH=> 317 494 1077

PR TYPE CODE(1)=> if INSTRUMENT TYPE CODE=> grt
(2)=> BASIS FOR SELECTION=> baa
(3)=> EQUIPMENT TITLE=>

BRANCH HEAD APPROVAL OF SOURCE JUST./RFP=> DATE=> ✓
BRANCH HEAD COMMENTS ON SOURCE JUSTIFICATIONS=>

SECTION LEADER USERID=> SECTION LEADER CODE=>
SECTION LEADER NAME=> , , .
DATE SECTION LEADER ASSIGNED=> ASSIGN WEIGHT=>

NEGOTIATOR USERID=> GALLMON NEGOTIATOR CODE=>
NEGOTIATOR NAME=> , , .
DATE NEGOTIATOR ASSIGNED=> 8-27
PREVIOUS NEGOTIATOR NAME=>Gallmon ,Julia ,M .
PCO USERID=> KURZIUS NAME=> CODE=>
S.O. NAME=>Yoder ,Max ,N .
S.O. USERID=>yoder S.O. CODE=>1114SS

TOTAL CUMULATIVE VALUE OF CURRENT CONTRACT=>305000 175000.00
TOTAL OBLIGATED FUNDING ON CURRENT CONTRACT=>175000 ~~358928.00~~
PREV NEG INCREMENTAL FUNDS PROVIDED BY THIS PR=>130000 ~~110000.00~~
NEW FUNDS BEING NEGOTIATED INTO CURRENT CONTRACT=> 0.00
CURRENTLY NEGOTIATED NEW FUNDS PROVIDED BY THIS PR=>0 ~~130000.00~~
TOTAL EXPECTED TO BE OBLIGATED ON FUTURE ACTIONS=> 0.00

FRC	PROGRAM YEAR	FUNDS INCREMENT	FS	FUNDS DUE DATE	ACRN	CSS FUNDS
4145	1991	130000.00	p	01 NOV 1990	AC	0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00

1498 TITLE=>(u)GaAs Gate Dynamic Memory Technology

REPORTS FREQUENCY CODE->sem

PI NAME=>Michael R Melloch
PI TELEPHONE=>(317) 494 3528 EXT=>

CONTRACT PROPOSAL/REQUISTION NUMBER=>

ONR PROPSOAL NUMBER=>

PATENTS INTEREST CODE=>

CLASSIFICATION DD 254=> DATE OF DD 254=>

Notes to 600:
This provides the final funding increment to the contract.

Short Work Statement:
Investigate materials, techniques, designs, and fabrication procedures leading to high speed memory circuits exhibiting apriori controlled threshold voltages having little deviation and extremely long refresh times.

Extended Work Statement:
Investigate MESFET and MODFET DRAM memories as per section IV (Statement of Work) of the proposal.

BPS:Submission,Eval,Cost/JA:Desc:

This proposal was received in response to the ONR announcement of research interest published in the COMMERCE BUSINESS DAILY of 28 APR 1988. Award is recommended based on evaluation of the proposal in accordance with the following criteria (BPS items 1-6):

Financial Considerations:

Labor -
The proposed quantities and types of labor (including any consultants and labor provided by subgrantee) are reasonable and necessary for accomplishing the research project.
The proposed labor rates are in line with standard academic or industrial practice for research of this type.
Any consulting at a rate in excess of $500.00 per day is justified in the "Additional Consultant Information" text item.

Other Direct Costs-
Other proposed direct costs (such as supplies, equipment, ADP, travel, etc.) are reasonable and necessary for accomplishing the research project.

I have reviewed and accepted the proposed budget subject to the grant/contracting office's verification of rates ir indirect costs. Where changes to the original budget were necessary have had

the principal investigator submit a revised budget through official university channels and that revised budget is enclosed. The proposal appears to be fair, reasonable, in the interest of the government, and is consistent with other previous and current efforts of this nature.

BPS:Overall Merits/JA:Contr Quals:
This work incorporates two novel ideas, synergistically combined. They are (a) a buried heterojunction charge storage well and (b) a semiconductor, zero interface state density FET gate separated by an undoped quantum barrier.

BPS:ONR Mission/JA:Enhance Comp:
If successful, this will result in the first GaAS dynamic Modfet random access memory. This should enable radiation hard memory technology operating at GHz clock speeds and with cell density 6 times that of present GaAs memories. Dense memories such as these will reduce interconnects among chips and improve military readiness and reliability.

BPS:Contr Quals/JA:Noncomp Justfctn:
The proposed contractor provides the unique capabilities and experience of the principal investigator as described in the research proposal. The principal investigator would not be available through any other contractor.

BPS:PI Quals/JA:Improve Comp:
The principal investigator is highly qualified to execute the proposed program based on his previous experience, publications, and presentations as described in the proposal.

1498 Technical Objective:
(U) This work seeks new low cost approaches to high speed memory required in future Navy signal processing systems.

1498 Approach:
(U) Buried heterojunction charge storage wells will be used in conjunction with semiconductor gates to create memory devices exhibiting very low (e.g., one hour) room temperature refresh times. MBE-grown aluminum arsenide and gallium arsenide will be used. Doped alloys will be avoided.

1498 Progress:
(U) Buried memory storage cells using the capacitance of a reversed biased P-N junction have been fabricated and tested. The cells include the associated storage cell transistor and the read and write transistors in the single cell memory "array". Storage times in excess of 0.5 minute at room temperature were achieved for the IC.

Accounting Classification

ACRN-FRC-PY-----APPN------SUBHD-OBJ-BCN-SA--AAA---TT--PAA----COST CODE-----PE--
4145 1991 1711319 .W1AE 000 RA414 0 068342 2B 000000 021020000100 0601153N
Funds Source Title: ONR1RDN
Source for Initialization: RPDP-5-91 CODE 111

Contractor Information:
Short Contractor Code: purd
Purdue Research Foundation
Division of Sponsored Programs
Hovde Hall, Third Floor
West Lafayette, IN 47907

Size & Type: ls
Country: US
City Code: 82862
State Code: 18
Duns Code: 070710447
DLA Milscap Code: 48877
Payment Dodaad Code: N00179
ACO Milscap Code: N62880
Cognizant Audit Agency: hs05
TIN: 351052049
PTIN:

PROJECT CODE=> 414f004---08 / PREV R & T PROJECT CODE=> 414f004---07
SUBMISSION DATE=> 16 AUG 1990
CONTRACTOR NAME=> Purdue Research Foundation
PR TYPE CODE=> if
SU CODE=> 414SS
ITC=> grt
STARS PR NO=> N0001491PR24595

FRC	PROGRAM YEAR	FUNDS INCREMENT	FUNDS EXPIRATION DATE	FS
4145	1991	130000.00	30 SEP 1991	P

1498 TITLE=>(u)GaAs Gate Dynamic Memory Technology

DO NOT EXECUTE
PR must be returned to Code 01122 for signatures prior to execution.
Released for execution by Code 01122 ..... date .....

lotes to 500:
lo Text Available.

otes to 600:
his provides the final funding increment to the contract.

:counting Classification

:RN-FRC-PY-----APPN------SUBHD-OBJ-BCN-SA--AAA---TT--PAA----COST CODE-----PE--
4145 1991 1711319 •WIAE 000 RA414 0 068342 2B 000000 021020000100 0601153N
nds Source Title: ONR1RDN
urce for Initialization: RPDP-5-91 CODE 111

ort Work Statement:
'estigate materials, techniques, designs, and fabrication procedures
ding to high speed memory circuits exhibiting apriori controlled
eshold voltages having little deviation and extremely long refresh
es.

ended Work Statement:
•stigate MESFET and MODFET DRAM memories as per section IV
ltement of Work) of the proposal.

DBue 8.23.90 (b) (6)

T. PROJECT CODE=> 414F004---08 PREV R & T PROJECT CODE=> 414F004---07
R SUBMISSION DATE=> 10 AUG 1990
CONTRACT NUMBER=> N00014891J1864 CONTRACT MOD NUMBER=> P00002
START DATE OF CURRENT CONTRACT=> 01 FEB 1989 END DATE=> 31 DEC 1991
REQUESTED START DATE=> 01 NOV 1990 END DATE=> 31 DEC 1991
NEGOTIATED START DATE=> 01 NOV 1990

CONTRACTOR NAME=> Purdue Research Foundation
SHORT CONTRACTOR CODE=> purd SIZE AND TYPE BUSINESS CODE=> 1s
CONTRACTOR STREET=> Hovde Hall, Third Floor
CONTRACTOR CITY=> West Lafayette
CONTRACTOR STATE=> IN CONTRACTOR ZIP CODE=> 47907
REP=> Chandrea Lightfoot PH=> 317 494 1077

PR TYPE CODE(1)=> if INSTRUMENT TYPE CODE=> grt
(2)=> BASIS FOR SELECTION=> baa
(3)=> EQUIPMENT TITLE=>

BRANCH HEAD APPROVAL OF SOURCE JUST./RFP=> DATE=> V
BRANCH HEAD COMMENTS ON SOURCE JUSTIFICATIONS=>

SECTION LEADER USERID=> SECTION LEADER CODE=>
SECTION LEADER NAME=> , , .
DATE SECTION LEADER ASSIGNED=> ASSIGN WEIGHT=>

NEGOTIATOR USERID=> GALLMON NEGOTIATOR CODE=>
NEGOTIATOR NAME=> , , .
DATE NEGOTIATOR ASSIGNED=> 8-27
PREVIOUS NEGOTIATOR NAME=>Gallmon ,Julia ,M .
PCO USERID=> KURZIUS NAME=> CODE=>
S.O. NAME=>Yoder ,Max ,N .
S.C. USERID=>yoder S.O. CODE=>11465

TOTAL CUMULATIVE VALUE OF CURRENT CONTRACT=>305000 ~~750000.00~~
TOTAL OBLIGATED FUNDING ON CURRENT CONTRACT=>175000 ~~353725.00~~
PREV NEG INCREMENTAL FUNDS PROVIDED BY THIS PR=>130000 ~~100000.00~~
NEW FUNDS BEING NEGOTIATED INTO CURRENT CONTRACT=> 0.00
CURRENTLY NEGOTIATED NEW FUNDS PROVIDED BY THIS PR=>0 ~~130000.00~~
TOTAL EXPECTED TO BE OBLIGATED ON FUTURE ACTIONS=> 0.00

FRC	PROGRAM YEAR	FUNDS INCREMENT	FS	FUNDS DUE DATE	ACRN	CSS FUNDS
4145	1991	130000.00	P	01 NOV 1990	AC	0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00

R & T PROJECT CODE=> 414f004---07 PREV R & T PROJECT CODE=> 414f004---06
PR SUBMISSION DATE=> 13 SEP 1989
CONTRACTOR NAME=> Purdue Research Foundation
PR TYPE CODE=> 1f
SO CODE=> 414SS
ITC-> grt
STARS PR NO=> N0001490PR24935

FRC	PROGRAM YEAR	FUNDS INCREMENT	FUNDS EXPIRATION DATE	FS
4145	1990	110000.00	30 SEP 1990	p 9.14.89 (b) (6)

1498 TITLE=>(u)GaAs Gate Dynamic Memory Technology

Notes to 500:
No Text Available.

Notes to 600:
No Text Available.

Accounting Classification

ACRN-FRC-PY-----APPN------SUBHD-OBJ-BCN-SA--AAA---TT--PAA----COST CODE-----PE--
4145 1990 1701319 .W1AE 000 RA414 0 068342 2B 000000 021020000100 0601153
Funds Source Title: ONR1RDN
Source for Initialization: RPDP-5-90 CODE 11

DO NOT EXECUTE
PR must be returned to Code 01122 for signatures prior to execution.
Released for execution by Code 01122 _____ date _____

R & T PROJECT CODE=> 414f004---07 PREV R & T PROJECT CODE=> 414f004---06
PR SUBMISSION DATE=> 13 SEP 1989
CONTRACT NUMBER=> N0001489J1864 CONTRACT MOD NUMBER=> P00001
START DATE OF CURRENT CONTRACT=> 01 FEB 1989 END DATE=> 31 DEC 1991
REQUESTED START DATE=> 01 NOV 1989 END DATE=> 31 DEC 1991
NEGOTIATED START DATE=> 01 NOV 1989

CONTRACTOR NAME=> Purdue Research Foundation
SHORT CONTRACTOR CODE=> purd SIZE AND TYPE BUSINESS CODE=> 1s
CONTRACTOR STREET=> Hovde Hall, Third Floor
CONTRACTOR CITY=> West Lafayette
CONTRACTOR STATE=> IN CONTRACTOR ZIP CODE=> 47907
REP=> Chandrea Lightfoot PH=> 317 494 1077

PR TYPE CODE(1)=> if INSTRUMENT TYPE CODE=> grt
(2)=> BASIS FOR SELECTION=> baa
(3)=> EQUIPMENT TITLE=>

BRANCH HEAD APPROVAL OF SOURCE JUST./RFP=> (b) (6) DATE=>
BRANCH HEAD COMMENTS ON SOURCE JUSTIFICATIONS=>

SECTION LEADER USERID=> Kurzius SECTION LEADER CODE=>
SECTION LEADER NAME=> , , .
DATE SECTION LEADER ASSIGNED=> ASSIGN WEIGHT=>

NEGOTIATOR USERID=> Gallmon NEGOTIATOR CODE=>
NEGOTIATOR NAME=> 10-30 , , .
DATE NEGOTIATOR ASSIGNED=>
PREVIOUS NEGOTIATOR NAME=>Moya ,Betti Sue , .
PCO USERID=> NAME=> Bennet CODE=>
S.O. NAME=>Yoder ,Max ,N .
S.O. USERID=>yoder S.O. CODE=>1114SS

TOTAL CUMULATIVE VALUE OF CURRENT CONTRACT=> 305000 ~~65000.00~~
TOTAL OBLIGATED FUNDING ON CURRENT CONTRACT=> 65000 ~~248928.00~~
PREV NEG INCREMENTAL FUNDS PROVIDED BY THIS PR=> 110000 ~~65000.00~~
NEW FUNDS BEING NEGOTIATED INTO CURRENT CONTRACT=> 0.00
CURRENTLY NEGOTIATED NEW FUNDS PROVIDED BY THIS PR=> 0 ~~110000.00~~
TOTAL EXPECTED TO BE OBLIGATED ON FUTURE ACTIONS=> 0.00

FRC	PROGRAM YEAR	FUNDS INCREMENT	FS	FUNDS DUE DATE	ACRN	CSS FUNDS
4145	1990	110000.00	p	01 NOV 1989	AB	0.00
4145	1991	130000.00		01 NOV 1990		0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00

1498 TITLE=>(u)GaAs Gate Dynamic Memory Technology

REPORTS FREQUENCY CODE=>sem

PI NAME=>Michael R Melloch
PI TELEPHONE=>(317) 494 3528 EXT=>

CONTRACT PROPOSAL/REQUISTION NUMBER=>

ONR PROPSOAL NUMBER=>

PATENTS INTEREST CODE=>

CLASSIFICATION DD 254=> DATE OF DD 254=>

Short Work Statement:
Investigate materials, techniques, designs, and fabrication procedures leading to high speed memory circuits exhibiting apriori controlled threshold voltages having little deviation and extremely long refresh times.

Extended Work Statement:
Investigate MESFET and MODFET DRAM memories as per section IV (Statement of Work) of the proposal.

BPS:Submission,Eval,Cost/JA:Desc:

This proposal was received in response to the ONR announcement of research interest published in the COMMERCE BUSINESS DAILY of 28 APR 1988. Award is recommended based on evaluation of the proposal in accordance with the following criteria (BPS items 1-6):

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Labor -
The proposed quantities and types of labor (including any consultants and labor provided by subgrantee) are reasonable and necessary for accomplishing the research project.
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the government, and is consistent with other previous and current efforts of this nature.

BPS:Overall Merits/JA:Contr Quals:
This work incorporates two novel ideas, synergistically combined. They are (a) a buried heterojunction charge storage well and (b) a semiconductor, zero interface state density FET gate separated by an undoped quantum barrier.

BPS:ONR Mission/JA:Enhance Comp:
If successful, this will result in the first GaAS dynamic Modfet random access memory. This should enable radiation hard memory technology operating at GHz clock speeds and with cell density 6 times that of present GaAs memories. Dense memories such as these will reduce interconnects among chips and improve military readiness and reliability.

BPS:Contr Quals/JA:Noncomp Justfctn:
The proposed contractor provides the unique capabilities and experience of the principal investigator as described in the research proposal. The principal investigator would not be available through any other contractor.

BPS:PI Quals/JA:Improve Comp:
The principal investigator is highly qualified to execute the proposed program based on his previous experience, publications, and presentations as described in the proposal.

1498 Technical Objective:
(U) This work seeks new low cost approaches to high speed memory required in future Navy signal processing systems.

1498 Approach:
(U) Buried heterojunction charge storage wells will be used in conjunction with semiconductor gates to create memory devices exhibiting very low (e.g., one hour) room temperature refresh times. MBE-grown aluminum arsenide and gallium arsenide will be used. Doped alloys will be avoided.

1498 Progress:
(U) The first integrated circuits using JFET readout and MESFET DRAM cells were fabricated in August 1989 and evaluated in September. Storage time between refresh was found to be 2 seconds. Refresh times of up to 15 minutes are envisioned with this technology. The technology uses no amorphous or polycrystalline insulators; as such, the DRAMs are expected to be extremely radiation tolerant, but radiation tests have not been made.

Accounting Classification

ACRN-FRC-PY-----APPN------SUBHD-OBJ-BCN-SA--AAA---TT--PAA----COST CODE-----PE--
4145 1990 1701319 .W1AE 000 RA414 0 068342 2B 000000 021020000100 0601153
Funds Source Title: ONR1RDN
Source for Initialization: RPDP-5-90 CODE 11

Contractor Information:
Short Contractor Code: purd
Purdue Research Foundation
Division of Sponsored Programs
Hovde Hall, Third Floor
West Lafayette, IN 47907

Size & Type: 1s
Country: US
City Code: 82862
State Code: 18
Duns Code: 070710447
DLA Milscap Code: 48877
Payment Dodaad Code: N00179
ACO Milscap Code: N62880
Cognizant Audit Agency: hs05

R & T PROJECT CODE	414f004---06
PREV R & T PROJECT CODE	414f004---05
PR SUBMISSION DATE	09 NOV 1988
CONTRACTOR NAME	Purdue Research Foundation
PR TYPE CODE	re
SO CODE	414SS
ITC	grt
STARS PR NO	N0001489PR24c33

PRC	PROGRAM YEAR	FUNDS INCREMENT	FUNDS EXPIRATION DATE	FS
4145	1989	65000.00	30 SEP 1989	

11/15/88 (b) (6)

1498 TITLE (U)GaAs Gate Dynamic Memory Technology

Notes to 500:
No Text Available.

Notes to 600:
There is no capitol equipment in this procurement. Approved by T.Arnold:
Although the proposal for this renewal procurement gives a starting date of 01 June 1989 commensurate with the end date of the present contract, Purdue would actually like the start date of the renewal to begin earlier but still end on 31 December 1991. This will enable them to better prepare for committments to graduate students and give them more flexibility over expenditure rates. Accordingly, 01 Feb 89 is proposed.

Accounting Classification

ACRN-FRC-PY-----APPN-------SUBHD-OBJ-BCN-SA--AAA---TT--PAA-----COST CODE-----PE--
4145 1989 1791319 -W1AE 000 RA414 0 068342 2B 000000 021020000100 0601153
Funds Source Title: ONR1RDN
Source for Initialization: RPDP-7-89 - CODE 111

R & T PROJECT CODE 414f004---06 PREV R & T PROJECT CODE 414f004---05
PR SUBMISSION DATE 09 NOV 1988 89-J-1864
CONTRACT NUMBER ~~N000-1486K0350~~ CONTRACT MOD NUMBER ~~P00004~~
START DATE OF CURRENT CONTRACT 01 JUN 1986 END DATE 31 MAY 1989
REQUESTED START DATE 01 FEB 1989 END DATE 31 DEC 1991
NEGOTIATED START DATE 01 Feb 1989

CONTRACTOR NAME Purdue Research Foundation
SHORT CONTRACTOR CODE purd SIZE AND TYPE BUSINESS CODE 1s
CONTRACTOR STREET Hovde Hall, Third Floor
CONTRACTOR CITY West Lafayette
CONTRACTOR STATE IN CONTRACTOR ZIP CODE 47907
REP Chandrea Lightfoot PH 317 494 1077

PR TYPE CODE (1) re INSTRUMENT TYPE CODE grt
(2) if BASIS FOR SELECTION baa
(3) EQUIPMENT TITLE

BRANCH HEAD APPROVAL OF SOURCE JUST./RFP (b) (6) DATE 1-12-89
BRANCH HEAD COMMENTS ON SOURCE JUSTIFICATIONS
SEE NOTES TO 600

SECTION LEADER USERID SECTION LEADER CODE
SECTION LEADER NAME , , -
DATE SECTION LEADER ASSIGNED ASSIGN WEIGHT

NEGOTIATOR USERID [redacted] MOYA NEGOTIATOR CODE
NEGOTIATOR NAME , , -
DATE NEGOTIATOR ASSIGNED 1-12-89
PREVIOUS NEGOTIATOR NAME Ford ,Elizabeth , -
PCO USERID NAME CODE
S.O. NAME Yoder 64218 ,Max ,N -
S.O. USERID yoder S.O. CODE 1114SS

TOTAL CUMULATIVE VALUE OF CURRENT CONTRACT	~~271928.00~~
TOTAL OBLIGATED FUNDING ON CURRENT CONTRACT	~~183928.00~~
PREV NEG INCREMENTAL FUNDS PROVIDED BY THIS PR	0.00
NEW FUNDS BEING NEGOTIATED INTO CURRENT CONTRACT	305000.00 ok
CURRENTLY NEGOTIATED NEW FUNDS PROVIDED BY THIS PR	65000.00 ok
TOTAL EXPECTED TO BE OBLIGATED ON FUTURE ACTIONS	0.00

FRC	PROGRAM YEAR	FUNDS INCREMENT	FS	FUNDS DUE DATE	ACRN	CSS FUNDS
4145	1989	65000.00	a	01 FEB 1989	NA	0.00
4145	1990	110000.00		01 NOV 1989		0.00
4145	1991	130000.00		01 NOV 1990		0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00
		0.00				0.00

1498 TITLE (u)GaAs Gate Dynamic Memory Technology

REPORTS FREQUENCY CODE sem

PI NAME Michael R Melloch
PI TELEPHONE (317) 494 3523 EXT

CONTRACT PROPOSAL/REQUISTION NUMBER

ONR PROPSOAL NUMBER 89414---0028

PATENTS INTEREST CODE

CLASSIFICATION DD 254 DATE OF DD 254

Notes to 600:
There is no capitol equipment in this procurement. Approved by T.Arnold: Although the proposal for this renewal procurement gives a starting date of 01 June 1989 commensurate with the end date of the present contract, Purdue would actually like the start date of the renewal to begin earlier but still end on 31 December 1991. This will enable them to better prepare for committments to graduate students and give them more flexibility over expenditure rates. Accordingly, 01 Feb 89 is proposed.

Short Work Statement:
Investigate materials, techniques, designs, and fabrication procedures leading to high speed memory circuits exhibiting apriori controlled threshold voltages having little deviation and extremely long refresh times.

Extended Work Statement:
Investigate MESFET and MODFET DRAM memories as per section IV (Statement of Work) of the proposal.

BPS:Submission,Eval,Cost/JA:Desc:

This proposal was received in response to the ONR announcement of research interest published in the COMMERCE BUSINESS DAILY of 28 APR 1988. Award is recommended based on evaluation of the proposal in accordance with the following criteria (BPS items 1-6):

Financial Considerations:

Labor -
The proposed quantities and types of labor (including any consultants and labor provided by subgrantee) are reasonable and necessary for accomplishing the research project.
The proposed labor rates are in line with standard academic or industrial practice for research of this type.
Any consulting at a rate in excess of $500.00 per day is justified in the "Additional Consultant Information" text item.

Other Direct Costs-
Other proposed direct costs (such as supplies, equipment, ADP,

travel, etc.) are reasonable and necessary for accomplishing the research project.

I have reviewed and accepted the proposed budget subject to the grant/contracting officer's verification of rates in indirect costs. Where changes to the original budget were necessary I have had the principal investigator submit a revised budget through official university channels and that revised budget is enclosed. The proposal appears to be fair, reasonable, in the interest of the government, and is consistent with other previous and current efforts of this nature.

BPS:Overall Merits/JA:Contr Quals:
This work incorporates two novel ideas, synergistically combined. They are (a) a buried heterojunction charge storage well and (b) a semiconductor, zero interface state density FET gate separated by an undoped quantum barrier.

BPS:ONR Mission/JA:Enhance Comp:
If successful, this will result in the first GaAS dynamic Modfet random access memory. This should enable radiation hard memory technology operating at GHz clock speeds and with cell density 6 times that of present GaAs memories. Dense memories such as these will reduce interconnects among chips and improve military readiness and reliability.

BPS:Contr Quals/JA:Noncomp Justfctn:
The proposed contractor provides the unique capabilities and experience of the principal investigator as described in the research proposal. The principal investigator would not be available through any other contractor.

BPS:PI Quals/JA:Improve Comp:
The principal investigator is highly qualified to execute the proposed program based on his previous experience, publications, and presentations as described in the proposal.

1498 Technical Objective:
(U) This work seeks new low cost approaches to high speed memory required in future Navy signal processing systems.

1498 Approach:
(U) Buried heterojunction charge storage wells will be used in conjunction with semiconductor gates to create memory devices exhibiting very low (e.g., one hour) room temperature refresh times. MBE-grown aluminum arsenide and gallium arsenide will be used. Doped alloys will be avoided.

1498 Progress:
(U) Room temperature storage times of over 90 minutes have been demonstrated in III-V MODFET comprisel of an n-type storage region surrounded by p-type material of a higher bandgap. In contrast to many other types of storage type memories, the leakage of the controlling transistor in this device does NOT discharge the storage media.

Accounting Classification

ACRN-FRC-PY-----APPN------SUBHD-OBJ-SCN-SA--AAA---TT--PAA----COST CODE-----PE--
4145 1989 1791319 .W1AE 000 RA414 0 068342 2B 000000 021020000100 0601153
Funds Source Title: ONR1RDN

Source for Initialization: RPDP-7-89 - CODE 111

Contractor Information:
Short Contractor Code: purd
Purdue Research Foundation
Division of Sponsored Programs
Hovde Hall, Third Floor
West Lafayette, IN 47907

Size & Type: 1s
Country: US
City Code: 82862
State Code: 18
Duns Code: 070710447
DLA Milscap Code: 4B877
Payment Dodaad Code: N00179
ACO Milscap Code: N62880
Cognizant Audit Agency: hs05

PURDUE RESEARCH FOUNDATION

DIVISION OF
SPONSORED PROGRAMS

REF: DSP #K259 March 22, 1989

Office of Naval Research
Attn: Betty Moya, Code 1513
800 N. Quincy St.
Arlington, VA 22217 5000

Subject: Proposal Entitled, "GaAs Gate Dynamic Memory Technology"
Task No. 414F004---06
Project Director: M. R. Melloch, Purdue

Dear Ms. Moya:

Enclosed please find the additional information you requested for the subject proposal. A starting grant date of 2/1/89 is acceptable to Purdue Research Foundation.

If you have any questions, please contact Mr. Tom Wright, at telephone 317/494-1078.

Sincerely,

(b) (6)

Keven Anne Gipson
Proposal Supervisor
Division of Sponsored Programs

Enclosure

Supplies

06/01/89 to 05/31/90

Chemical Materials (TCE, Acetone, Methanol Hydrogen Peroxide, Sulfuric Acid, Hydrochloric Acid, Ammonium Hydroxide, Nitric Acid, Photoresist)	$ 500
GaAs substrates 20 - 2-inch wafers	$3,000
Liquid Nitrogen (for pumps and as source of pure nitrogen gas)	$ 500
Electron beam photoplates and supplies	$1,000
Molecular Beam Epitaxy System Source Material (Arsenic, Gallium, and Aluminum)	$1,000
TOTAL	$6,000

06/01/90 to 05/31/91

Chemical Materials (TCE, Acetone, Methanol, Hydrogen Peroxide, Sulfuric Acid, Hydrochloric Acid, Ammonium Hydroxide, Nitric Acid)	$ 500
GaAs Substrates 20 - 2-inch wafers	$3,000
Liquid Nitrogen (for pumps and as source of pure nitrogen gas)	$ 500
Electron beam photoplates and supplies	$1,000
Molecular Beam Epitaxy System Source Material (Arsenic, Gallium, and Aluminum)	$1,000
TOTAL	$6,000

06/01/91 to 12/31/91

Chemical Materials (TCE, Acetone, Methanol, Hydrogen Peroxide, Sulfuric Acid, Hydrochloric Acid, Ammonium Hydroxide, Nitric Acid)	$ 300
GaAs substrates 15 - 2-inch wafers	$2,250
Liquid Nitrogen (for pumps and as source of pure nitrogen gas)	$ 250
Electron beam photoplates and supplies	$ 200
Molecular Beam Epitaxy System Source Material (Arsenic, Gallium, and Aluminum)	$ 500
TOTAL	$3,500

Expendable Equipment

06/0189 to 05/31/90	
60 cc pyrolytic boron nitride crucible part # H6830 from Union Carbide Corporation	$ 800
Nude Ion Gauge filament Part # 971-0018 from Varian Associates, Inc.	$ 136
3 - Nanopure Expendables Kit (D3804) from Curtis Mathes Scientific, Inc.	$ 725
Replacement Gauge for beam flux monitor, Part # 663396 from Varian Associates, Inc.	$ 550
Nude Ion Gauge, Part # 971-5008 from Varian Associates, Inc.	$ 289
TOTAL	$2,500
06/01/90 to 05/31/91	
Reflection Electron Diffraction Phosphorescence Screen, Part # 981-3357 from Varian Associates, Inc.	$1,750
3 - Nanopure Expendables Kit (D3804) from Curtis Mathes Scientific, Inc.	$ 725
High Tack Mats, Part # C1631 from Lab Safety Supply	$ 25
TOTAL	$2,500
06/01/91 to 12/31/91	
4 - High Tack Mats, Part # C1631 from Lab Safety Supply Co.	$ 83
3 - Nanopure Expendables Kits (D3804) from Curtis Mathes Scientific, Inc.	$ 725
Nude ion gauge filament, Part # 971-0018 from Varian Associates, Inc.	$ 136
1 J-3400-00 Hot Plate (H2260-1) from Scientific Products	$ 77
Ti-Ball sublimation source, Part # 916-0005 from Varian Associates, Inc.	$ 451
Titanian sublimation pump filaments, Part # 916-0024 from Varian Associates, Inc.	$ 228
TOTAL	$1,700

Travel

06/01/89 to 05/31/90

Device Research Conference and Electronic Materials Conference at MIT, June 19-23, 1989

Air fare	$165/ea x 3 people	$ 495.00
Taxi		$ 62.00
Registration	$100 x 3 people	$ 300.00
Lodging	$95/night x 3 nights x 3 people	$ 855.00
Subsistence	$24/day x 4 days x 3 people	$ 288.00
TOTAL		$2,000.00

06/01/90 to 05/31/91

1990 Workshop on Compound Semiconductor Materials and Devices, West Coast

Air fare	$395/ea x 2 people	$ 790.00
Taxi	$22/ea x 2 people x 2 trips	$ 88.00
Registration	$130 x 2 people	$ 260.00
Lodging	$120/night x 3 nights x 2 people	$ 720.00
Subsistence	$24/day x 4 days x 4 people	$ 192.00
TOTAL		$2,050.00

06/01/91 to 12/31/91

1991 Electron Devices Meeting, Washington, DC

East Coast Symposium:

Air fare	$439/ea x 1 people	$ 439.00
Taxi	$20/ea x 1 people x 2 trips	$ 40.00
Registration	$150 x 1 people	$ 150.00
Lodging	$125/night x 3 nights x 1 people	$ 375.00
Subsistence	$24/day x 4 days x 1 people	$ 96.00
TOTAL		$1,100.00

Publications

06/01/89 to 05/31/90

Four - three page articles in Applied Physics Letters at $20 per article and $85 per page	$1,100

06/01/90 to 05/31/91

Four - three page articles in Applied Physics Letters at $20 per article and $85 per page	$1,100

06/01/91 to 12/31/91

Two - three page articles in Applied Physics Letters at $20 per article and $85 per page	$ 550

SHORT FORM RESEARCH CONTRACT
RESEARCH PROPOSAL COVER PAGE

Code 15 89414--0028
4147004---06

DATE SUBMITTED

DO NOT USE THIS BLOCK

1 TO (Submit copies of proposal to)	2 FROM (Name and address of offeror)
a NAME Max Yoder	a NAME Purdue Research Foundation
b ADDRESS (Street, City, State, Zip) Office of Naval Research Electronics Division, Code 414 Arlington, Virginia 22217-5000	b ADDRESS (Street, City, State, Zip) Hovde Hall, 3rd Floor W. Lafayette, Indiana 47907
	c IDENTIFICATION NUMBER
3 SCIENTIFIC FIELD Solid State Devices	4 TYPE OF ORGANIZATION (X one) X a. Educational Institution b. Other nonprofit
5 TITLE OF PROPOSAL GaAs Gate Dynamic Memory Technology	6 PROPOSAL ALSO BEING SUBMITED TO
7 PROPOSED AMOUNT $ 305,000	8. REQUESTED DURATION 2.5 years
9 REQUESTED START DATE (YYMMDD) 06/01/89	10 TYPE OF CONTRACT (X one) a Cost Plus Fixed Fee X b Cost, No Fee c Cost Sharing
11 PROPOSAL VALID UNTIL (Minimum 6 months) 12/01/89	

12 PRINCIPAL INVESTIGATOR(S)

a Name	b Department	c Telephone Number
(1) Michael R. Melloch	Electrical Engineering	317-494-3528
(2) James A. Cooper, Jr.	Electrical Engineering	317-494-3514
(3)		

13 ADMINISTRATIVE REPRESENTATIVE AUTHORIZED TO CONDUCT NEGOTIATIONS

a Name	b Department	c Telephone Number
(1) Tom Wright	Office of Contract & Grant Business Affairs	(317) 494- 1078
(2) Larry E. Pherson	Office of Contract & Grant Business Affairs	(317) 494- 1063

14 OFFEROR'S STATEMENTS (See Page 2) (Write enclosures or page numbers in appropriate block. If page numbers, precede item(s) by "pg.")

a Technical

pg 2	(1) Title and abstract of proposed effort
pg 6	(2) Statement of Work
pg 3	(3) Discussion of background, objectives, approaches, and available facilities
pg 17	(4) Names and brief biographical information of key personnel

b Financial

pg 32	(1) Cost estimate detailed by cost elements on SF 1411 or equivalent
	(2) Type of support other than financial, if any, required of the Government, e.g., facilities, equipment, materials, or personnel resources

c Administrative

	(1) Statements, if applicable, regarding cost sharing, organizational conflicts of interest, status of security clearances, environmental impact, and previous or organizational experience in the field covered by the proposal
	(2) Statement as to why it is necessary to acquire property, if any, with contract funds (See FAR 45.302)

15 AUTHORIZED REPRESENTATIVE

PURDUE RESEARCH FOUNDATION

a. Typed Name Robert A. Greenkorn	b Signature (b) (6) [redacted]
c. Title Vice President for Programs	d Date Signed (YYMMDD) October 25, 1988

DD Form 2222-2, 84 APR

Previous editions are obsolete

14. OFFEROR'S STATEMENTS

a. USE AND DISCLOSURE OF DATA *(X one)*

	(1) Except as indicated in (2) below, the proposal shall not be duplicated, used, or disclosed outside the Government in whole or in part for any purpose other than to evaluate the proposal without the written permission of the offeror (Except that if a contract is awarded on the basis of this proposal, the terms of this contract shall control disclosure and use) This restriction does not limit the Government's right to use information contained in the proposal if it is obtainable from another source without restriction. All data contained in this proposal is subject to this restriction unless specifically excluded by the offeror. The proposal has been marked as prescribed in FAR 15.509.
X	(2) Permission is hereby granted to evaluate this proposal in accordance with your normal procedures which may include evaluation by evaluators both within and outside the Government with the understanding that written agreement not to disclose this information shall not be required of or obtained from any such evaluators.

b. CONTRACT CLAUSES

By signature on Page 1 of this Proposal, the offeror authorizes award of a contract in accordance with the provisions of DFARS 35.70 and agrees to be bound by the contract clauses contained in DFARS 52.235-7005, in effect on the date of this proposal, or such other date as may be mutually agreed upon.

c. REPRESENTATIONS AND CERTIFICATIONS *(X one)*

X	(1) Representations and Certifications pertaining to Contingent Fee Representation and Agreement, Certification of Nonsegregated Facilities, Previous Contract Compliance Reports, Affirmative Action Compliance, and Clear Air and Water Certification, Organizational Conflicts of Interest, and Insurance Immunity From Tort Liability were furnished your office on *(Enter date)* 8/13/85. These representations and certifications remain valid and are appropriate for the subject proposal. No facility to be used for the proposed research has been the subject of a conviction under the Clean Air Act or the Federal Water Pollution Act.
	(2) The comprehensive Representations and Certifications as cited above have not been submitted. The attached Representations and Certifications have been developed in connection with the subject proposal and *(X one)*
	(a) should be used only in connection with the subject proposal.
	(b) may be used not only for the subject proposal but as a comprehensive submission for possible use with prospective unsolicited proposals..

d. ADVANCE PAYMENTS *(Applicable only to offerors with existing payment agreements with DOD)*

Advance payments will be made for performance of this SFRC pursuant to the terms and conditions of the Advance Payment Pool Agreement dated *(Enter date)* _____ between the Department of *(Enter name)* _____ and the contractor, *(Enter name)* _____ _____. The provisions of that Agreement are hereby incorporated by reference in this SFRC with the same force and effect as though fully set forth herein. If this SFRC is awarded by the Department that entered into the Advance Payment Pool Agreement with the Contractor, this SFRC shall be paid by *(Enter name and address of paying officer designated by the agreement)* _____ _____ _____ and deemed a "designated pool contract" for the purpose of said Agreement. If this SFRC contract is awarded by one of the other military departments or the Defense Logistics Agency, it will be deemed a "pool contract" for the purpose of said Agreement and, notwithstanding other provisions of this SFRC, all payments hereunder will be by check drawn payable to the dual payee, "Department of the *(Enter name)* _____ or *(Enter name of contractor)* _____ _____ " and forwarded to *(Enter name and address of paying office designated by the Agreement.)* _____ _____ _____ for appropriate disposition.

Table of Contents

GaAs Gate Dynamic Memory Technology

M. R. Melloch
J. A. Cooper, Jr.
School of Electrical Engineering
Purdue University
West Lafayette, IN 47907

Abstract

Under ONR support, during the last three years we have demonstrated the feasibility of building one-transistor dynamic random access memories (DRAMs) in GaAs. These memories are capable of operating over the temperature range to 125 C with storage times comparable or superior to silicon DRAMs. In this continuation proposal, we extend this work to demonstrate practical memory arrays in GaAs. We will investigate several options for building such arrays, including MESFET-, JFET-, and MODFET-isolated cells. We will identify the dominant leakage mechanisms in each type of cell, and optimize the cell and access transistor to minimize leakage, maximize storage capacity per unit area, and maximize speed of operation.

I. Objective

GaAs digital circuits are of interest because of their higher speed and lower power dissipation relative to silicon, their broader temperature range of operation, and their greater radiation tolerance. These factors make GaAs circuits very attractive for many military applications. There is a growing commercial market for digital GaAs as well, mainly in the area of high speed supercomputers. We believe future applications will also develop around the basic compatibility of GaAs with MMIC and optoelectronic devices.

Digital systems invariably require large amounts of memory, preferably integrated on the same chip with the processing elements. Recent studies of computer architecture for GaAs show that the speed advantage of GaAs microprocessors is severely compromised by the need to go off-chip for memory access. This is especially true since the off-chip/on-chip cycle time ratio is larger for GaAs circuits than for silicon (in other words, since GaAs systems are running faster than silicon, a long wait for off-chip access wastes more cycles in a GaAs system than a silicon system). This intensifies the need for fast, dense on-chip memory for GaAs digital systems. The one transistor dynamic RAM (DRAM) is the smallest, most dense semiconductor memory available. The availability of high density DRAM arrays in GaAs will have an enormous impact on the performance of GaAs digital systems by reducing the need for off-chip access, thereby directly improving the performance of the system as a whole.

The objective of this research is to demonstrate, characterize, and optimize dynamic RAM cells and prototype DRAM arrays for GaAs integrated circuits. As will be discussed below, we have already shown that one transistor DRAM cells can be built in GaAs with storage times comparable to those in silicon over the temperature range to 125 C. The proposed research will extend this work by optimizing the cell and access transistor combination to maximize (a) storage time, (b) charge storage capacity, and (c) speed, while (d) minimizing area. The scope of this work will encompass several cell geometries, including cells compatible with MESFET/JFET technology and with MODFET (HEMT) technology.

II. Background and Past Progress

Under an existing ONR contract, our group has been investigating the feasibility of constructing a one-transistor dynamic memory in GaAs. Dynamic memory cells can be grouped into two major categories: leakage-limited cells and generation-limited cells. In leakage-limited cells, information is stored by placing a greater-than-equilibrium number of electrons in a storage region. Information is lost when these excess electrons leak out of the cell by any of various mechanisms. We have found that leakage limited cells are generally restricted to operation at cryogenic temperatures, since it is difficult to construct an effective electron barrier in the AlGaAs/GaAs material system due to the small conduction band discontinuities available.

In generation-limited memories, information is stored by removing electrons from the storage region so that less than the equilibrium density of electrons is present. Information is lost as electrons are supplied to the cell by thermal generation. This is

the type of memory cell usually employed in silicon dynamic RAMs. We have found that in GaAs the thermal generation rate of electron-hole pairs is actually lower than in silicon at a comparable temperature, so that generation limited memories in GaAs will have even longer storage times than their silicon counterparts. We have demonstrated storage times of over 3 minutes at room temperature in all-GaAs cells and over 90 minutes at room temperature in cells constructed of $Al_{0.2}Ga_{0.8}As$. Both cells should be capable of operation up to 125 C.

The results described above were obtained using a cell in which electrons are stored on an n-type region in GaAs surrounded by p-type material, in effect a reverse biased pn junction. This structure is shown in Fig. 1. In order to form a one-transistor cell, it is necessary to connect this storage region to an access transistor. One simple way to do this is shown in Fig. 2. Here we have formed an n-channel JFET adjacent to the storage cell. Information can be written into the cell by biasing the access FET on and taking the source of the access transistor to a positive potential, thus withdrawing electrons from the storage region. To store information, the access transistor is turned off, isolating the storage region.

An array of storage cells is shown in Fig. 3. The gates of the access transistors are connected to a common horizontal word line, and the sources are connected to a common vertical bit line. The memory is word organized, and access is achieved by selecting a word line and reading out the stored information on all bits in that word in parallel on the bit lines. To read information out, the bit lines are first precharged to a known potential by a precharge transistor. The precharge transistors are then turned off, leaving the bit lines floating. The appropriate word line is turned on, connecting the selected storage bits to their corresponding bit lines. Charge now flows between the floating bit lines and the selected storage cells, altering the potential on the bit lines. Sense amplifiers connected to each bit line detect this change in potential, thereby reading the state of information in the storage cells.

One concern in constructing the FET-access storage cell is the degree to which leakage in the access transistor contributes to loss of information in the cell. We have investigated this for the case of the JFET isolated storage cell of Fig. 2. Measurements on only a few cells have been made so far, but preliminary indications are that leakage in the access transistor does not seriously degrade the storage time. For instance, at room temperature, we have measured storage times of 40 seconds in FET isolated cells of the type in Fig. 2. This compares to 300 seconds for similar cells without the access transistor. While this represents a substantial reduction, there are as yet not enough statistics to judge whether this difference is due to the influence of the access transistor or is a statistical fluke arising from variations in storage times due to random defects in the film. At any rate, we regard the 40 second storage time as proof that the FET isolated cell is capable of operation at room temperature and above.

III. Technical Approach

The proposed work will deal exclusively with generation-limited storage cells. Within this category, there are two important structural options to be considered. These are (a). JFET/MESFET storage cells, and (b). MODFET (HEMT) storage cells.

The JFET storage cell has been described in the first section and is illustrated in Fig. 2. The MESFET storage cell is directly analogous to this cell, and is shown in Fig. 4. Here the top P+ layer is eliminated, and the gate of the access transistor is formed by the Schottky barrier between the metal and the N-type channel. The storage cell may optionally be covered by a grounded Schottky gate to increase the storage capacitance. The MESFET DRAM cell is of special interest because it can be fabricated without MBE growth, using only a standard ion-implanted GaAs MESFET process. In fact, the only modification to the production GaAs FET process used in most industrial foundries would be the addition of a P-type implant for the tub region, and the associated ohmic contact to the P-tub, as shown in Fig. 5. The storage cell shown here is essentially a MESFET with a floating drain region. A further simplification, shown in Fig. 6, could eliminate the need for the P-tub, allowing the memory to be constructed with NO changes or additions to the conventional MESFET process. Although several of these MESFET options are attractive from a fabrication point of view, it remains to be established whether they will have sufficiently low leakage to provide adequate storage times. The study of the leakage mechanisms is a primary objective of the proposed research.

The second structural category for generation limited DRAM cells is the MODFET (or HEMT) device. In the MODFET, ionized dopant atoms in the higher bandgap AlGaAs material contribute carriers to the lower bandgap GaAs layer, as shown in Fig. 7. In equilibrium, a two-dimensional electron gas (2DEG) will exist at the GaAs/AlGaAs interface. This structure can be used as a generation-limited memory. To store information, we remove the 2DEG by drawing the electrons off into a positively biased region. The limitation on storage time is then the rate at which electrons are thermally generated to resupply the 2DEG. Structure and operation is entirely analogous to the MESFET/JFET DRAM discussed earlier. A diagram of a one-transistor MODFET DRAM cell is shown in Fig. 8. Again, the major problem is to identify and quantify the dominant generation and leakage mechanisms, both in the cell itself and in the access transistor, and to optimize the cell for maximum storage time and minimum area.

In either type of generation-limited memory, it may be helpful to employ a surface chemical treatment to reduce electron-hole pair generation at exposed GaAs surfaces. Recently, significant reductions in dark current have been achieved in GaAs PN diodes using $(NH_4)_2S$ as a surface passivation. Moreover, unlike earlier reports of chemical treatments using Na_2S, $(NH_4)_2S$ appears to be stable in room air for long periods of time, and is insoluble to DI water rinse. In addition to treating etched edges and exposed surfaces of GaAs, it may be beneficial to apply the chemical treatments under the Schottky gate metal of MESFET access transistors. Recent work at Purdue has shown that treating the GaAs surface with $(NH_4)_2S$ prior to evaporation of Schottky metal reduces surface state density by an order of magnitude, thereby unpinning the Fermi level. As more is learned about the long term stability of chemical surface treatments, we may be able to use these techniques to further improve the storage time of DRAM cells.

IV. Statement of Work

The program tasks are expressed in outline form below. We envision parallel efforts on MESFET/JFET DRAM development (heading A below) and MODFET DRAM development (heading B below). Items marked with an asterisk have already been accomplished as of this writing, and are listed for information only.

A. MESFET DRAM Cell

1. Evaluate options for structure of cell *
   a. Buried PN junction, punchthrough isolated *
   b. Buried PN junction, FET isolated *
   c. Surface PN junction, FET isolated *
2. Study leakage mechanisms in cell *
   a. Generation in depletion region *
   b. Generation at edges of cell *
3. Investigate sub-threshold leakage in access transistor
   a. Develop 2-D electrostatic model for short-channel MESFET / JFET *
   b. Investigate effect of FET parameters on sub-V_T slope
   c. Investigate leakage from gate electrode and determine whether MESFET or JFET is optimum
4. Fabricate and test one-transistor MESFET / JFET DRAM cell
5. Design prototype memory array
   a. Design peripheral circuitry (word line drivers and bit line sense amps)
   b. Perform trial layout
   c. Perform SPICE simulation to evaluate performance
6. Fabricate and test prototype DRAM array

B. MODFET DRAM Cell

1. Evaluate options for structure of cell
   a. Gated or ungated storage cell
   b. Normal (AlGaAs) or superlattice (GaAs/AlAs) barrier
   c. Single or double heterojunction cell
2. Study leakage mechanisms in cell
   a. Generation in depletion region *
   b. Generation at edges of cell
3. Investigate sub-threshold leakage in access transistor
   a. Develop 2-D electrostatic model for short-channel MODFET *
   b. Investigate effect of FET parameters on sub-V_T slope
   c. Investigate leakage from gate electrode and determine whether metal or GaAs gate is optimum
4. Fabricate and test one-transistor MODFET DRAM cell
5. Design prototype memory array
   a. Design peripheral circuitry (word line drivers and bit line sense amps)
   b. Perform trial layout
   c. Perform SPICE simulation to evaluate performance
6. Fabricate and test prototype DRAM array

V. DRAM-Related Publications Acknowledging ONR Support

[1] R. L. Gunshor, L. A. Kolodziejski, M. R. Melloch, M. Vaziri, C. Choi, and N. Otsuka, "Nucleation and Characterization of Pseudomorphic ZnSe Grown on Molecular Beam Epitaxially Grown GaAs Epilayers" Appl. Phys. Lett. 50, 200 (1987).

[2] M. R. Melloch, J. A. Cooper, Jr., and Q-D. Qian, "Investigation of Minority Carrier Retention Behind AlAs Barriers," Journal of Vac. Sci. and Tech. B 5, (1987).

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[4] A. K. Arora, A. K. Ramdas, M. R. Melloch, and No. Otsuka, "Interface vibrational Raman lines in GaAs/Al_xGa_{1-x} As superlattices," Phys. Rev. B35, (1987).

[5] M. S. Carpenter, M. R. Melloch, M. S. Lundstrom, S. P. Tobin, "Effects of Na_2S and $(NH_4)_2S$ edge passivation treatments on the dark current-voltage characteristics of GaAs pn diodes," Appl. Phys. Lett. 52, 2157 (1988).

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[7] Q-D. Qian, M. R. Melloch, and J. A. Cooper, Jr., "Electrical Behavior of a Static Hole Inversion Layer at the i-AlAs/n-GaAs Heterojunction," Journal of Applied Physics.

[8] J. S. Kleine, Q-D. Qian, J. A. Cooper, Jr., and M. R. Melloch, "Electron Emission from Direct Bandgap Heterojunction Capacitors," submitted to IEEE Transactions on Electron Devices.

[9] B. A. Cowans, Z. Dardas, W. N. Delgass, M. S. Carpenter, and M. R. Melloch, "X-ray Photoelectron Spectroscopy of Ammonium Sulfide Treated GaAs (100) Surfaces," submitted to Applied Physics Letters.

[10] M. R. Melloch, J. A. Cooper, Jr., and Q-D. Qian, "Investigation of Minority Carrier Hole Retention Behind AlAs and AlAs/GaAs Superlattice Barriers," Seventh US MBE Workshop, Boston, MA, October 20-22, 1986.

[11] M. Vaziri, R. L. Gunshor, L. A. Kolodziejski, and M. R. Melloch, "Characterization of ZnSe on GaAs Epilayers," March Meeting of the American Physical Society, New York, New York, March 16-20, 1987.

[12] L. A. Kolodziejski, R. L. Gunshor, M. Melloch, M. Vaziri, C. Choi, and N. Otsuka, "MBE of ZnSe on GaAs Epilayers," SPIE's conference on Growth of Compound Semiconductors, Bay Point, Florida, March 26-27, 1987.

[13] G. S. Studtmann, R. L. Gunshor, L. A. Kolodziejski, M. R. Melloch, N. Otsuka, D. P. Munich, J. A. Cooper, and R. F. Pierret, "Pseudomorphic ZnSe/GaAs MISFET Devices," 45th Device Research Conference, University of California at Santa Barbara, June 22-24, 1987.

[14] T. E. Dungan, J. A. Cooper, Jr., and M. R. Melloch, "Room Temperature Dynamic Memories for GaAs Integrated Circuits," 1987 International Electron Devices Meeting Technical Digest, Washington, D.C., December 7-9, 1987.

[15] M. S. Carpenter, M. R. Melloch, and T. E. Dungan, "Formation of Schottky Barriers on Reduced Surface State GaAs," 1988 International Symposium on Gallium Arsenide and Related Compounds," Atlanta, Georgia, September 11-14, 1988.

[16] J. S. Kleine, Q-D. Qian, J. A. Cooper, Jr., and M. R. Melloch, "Mathematical Model for Carrier Emission from a Static Two-Dimensional Electron Gas," 1988 International Symposium on Gallium Arsenide and Related Compounds," Atlanta, Georgia, September 11-14, 1988.

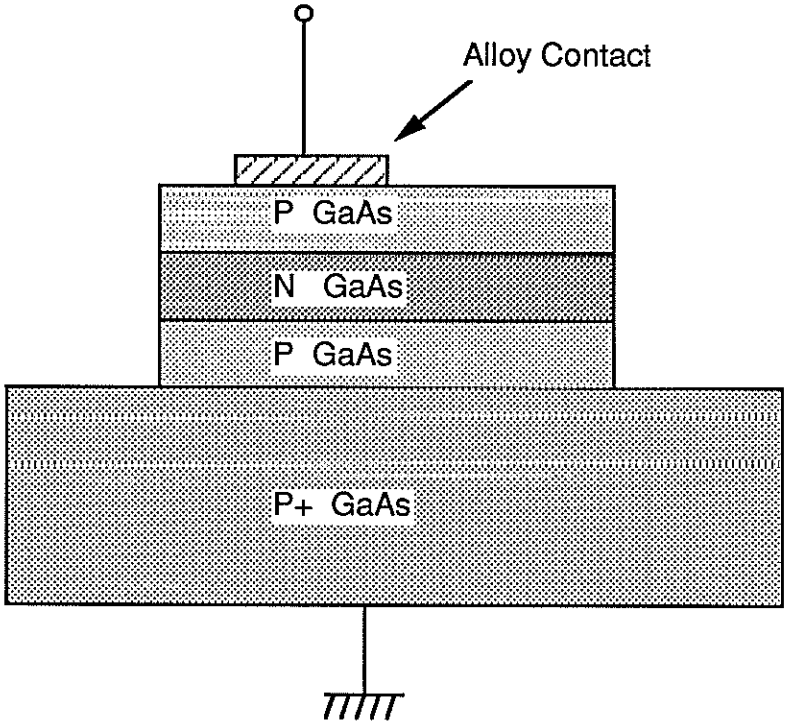

Figure 1. DRAM cell used to demonstrate feasibility of generation-limited memories in GaAs. Charge was stored on the N region and was isolated by the two reverse biased PN junctions. Storage times of 3 minutes at room temperature were obtained using this cell, in spite of the presence of etched edges at the periphery. Cell area was typically 300x300 μm.

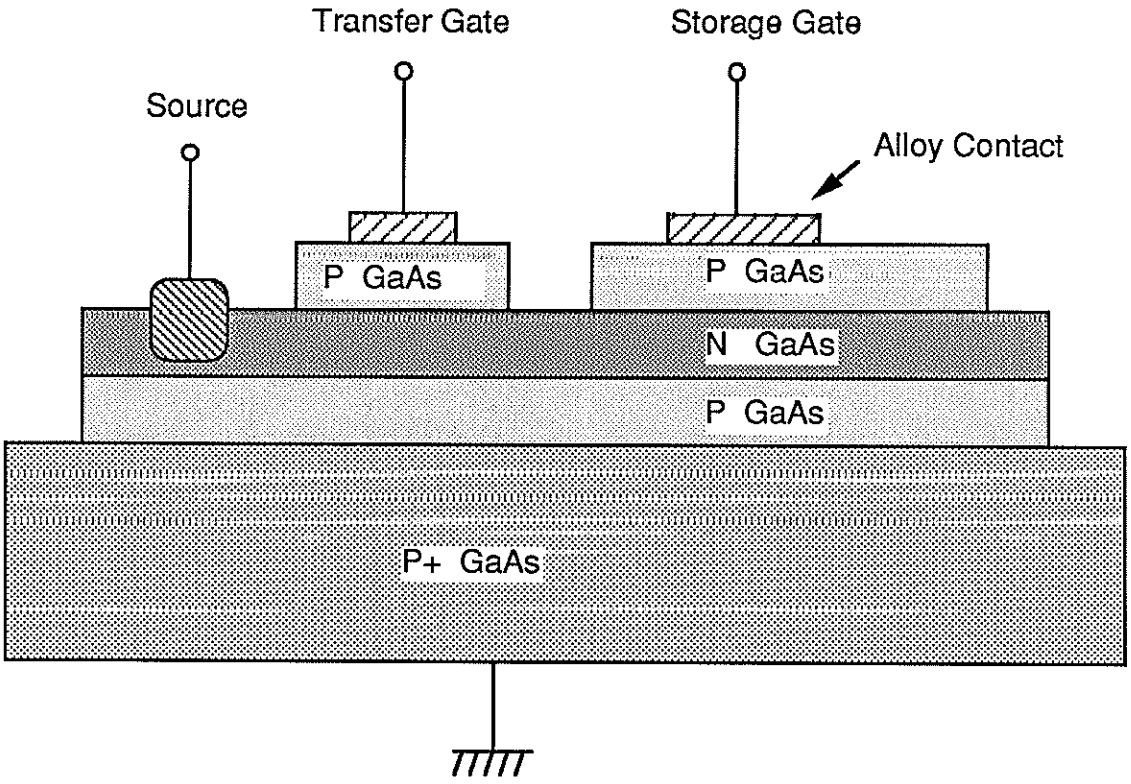

Figure 2. JFET-isolated DRAM cell. A preliminary version of this type of cell has demonstrated 40 second storage time at room temperature in spite of the additional leakage mechanisms inherent in the access transistor.

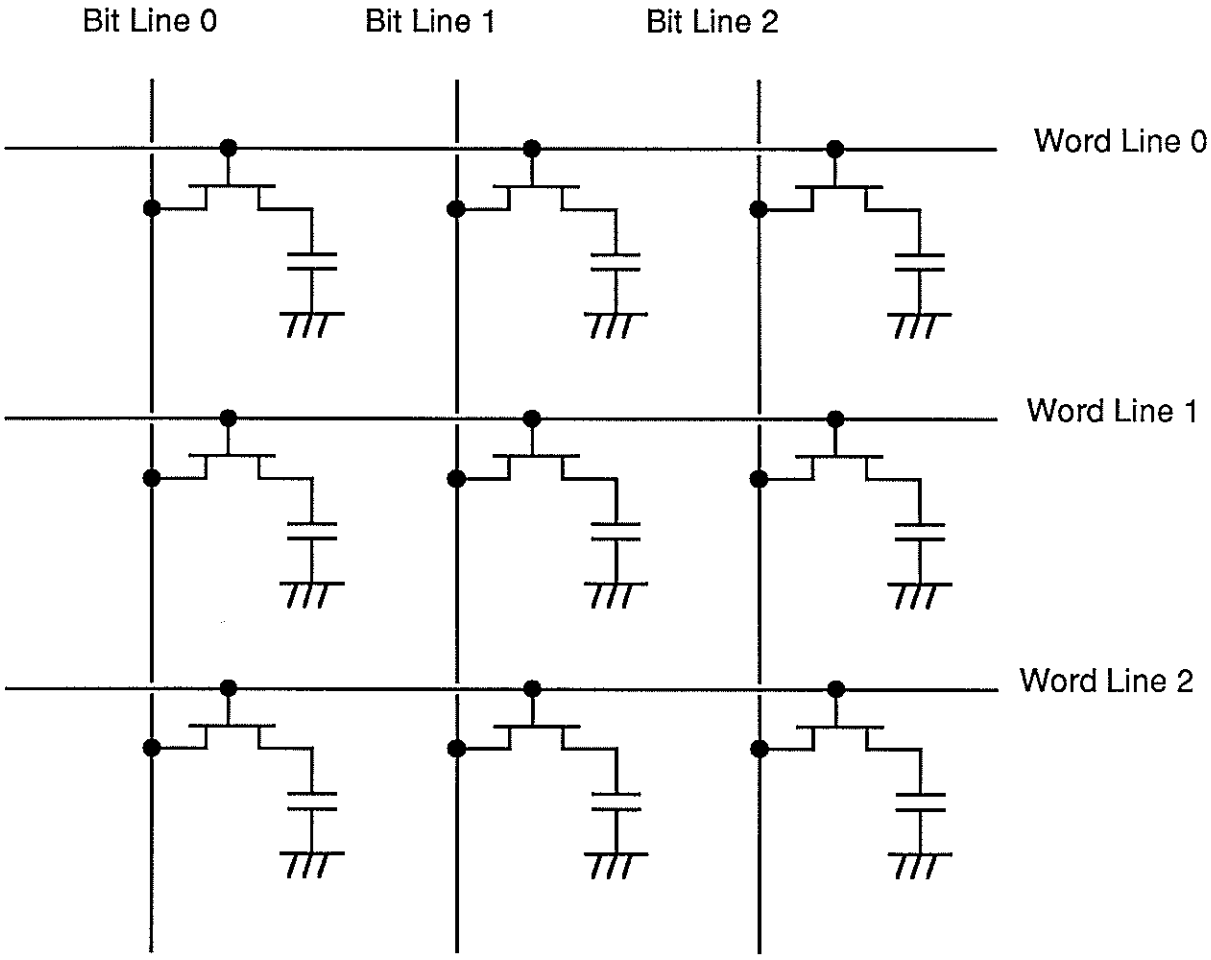

Figure 3. Example of a simple memory array containing nine dynamic storage cells. Addressing, precharge, and sensing circuits are located around the periphery, and are not shown in this figure.

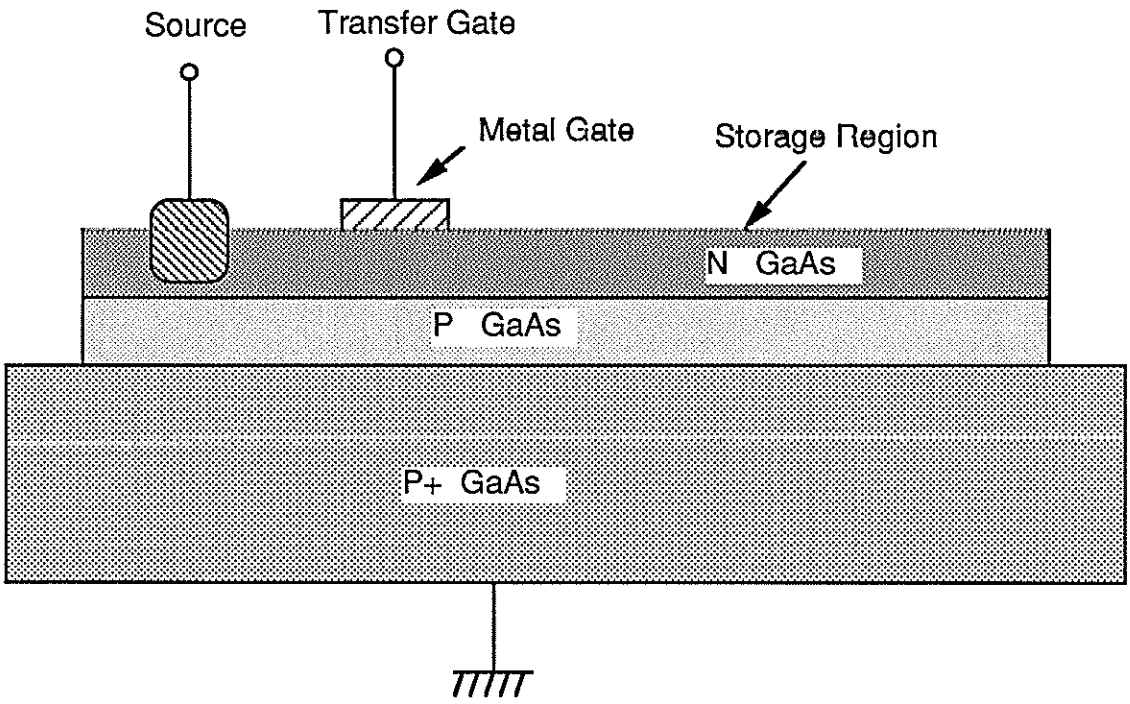

Figure 4. MESFET-isolated DRAM cell. A major objective of this research is to determine whether the MESFET access transistor and exposed top surface allow acceptable storage times.

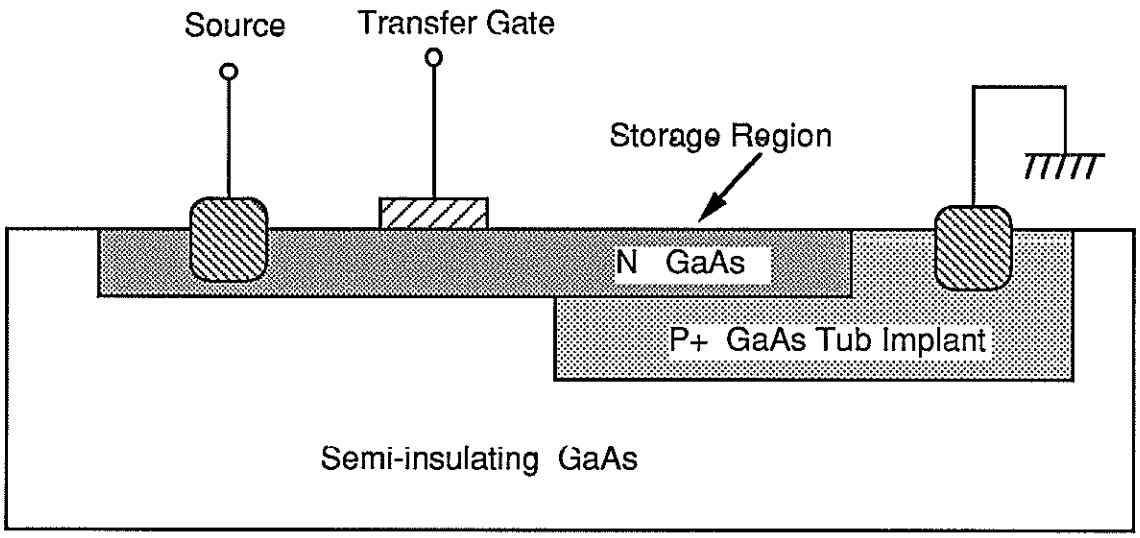

Figure 5. MESFET-isolated DRAM cell with ion-implanted P-tub. The P-tub forms a reverse-biased PN junction with the overlying N channel layer. Information is stored by reverse biasing this junction and turning the access transistor off.

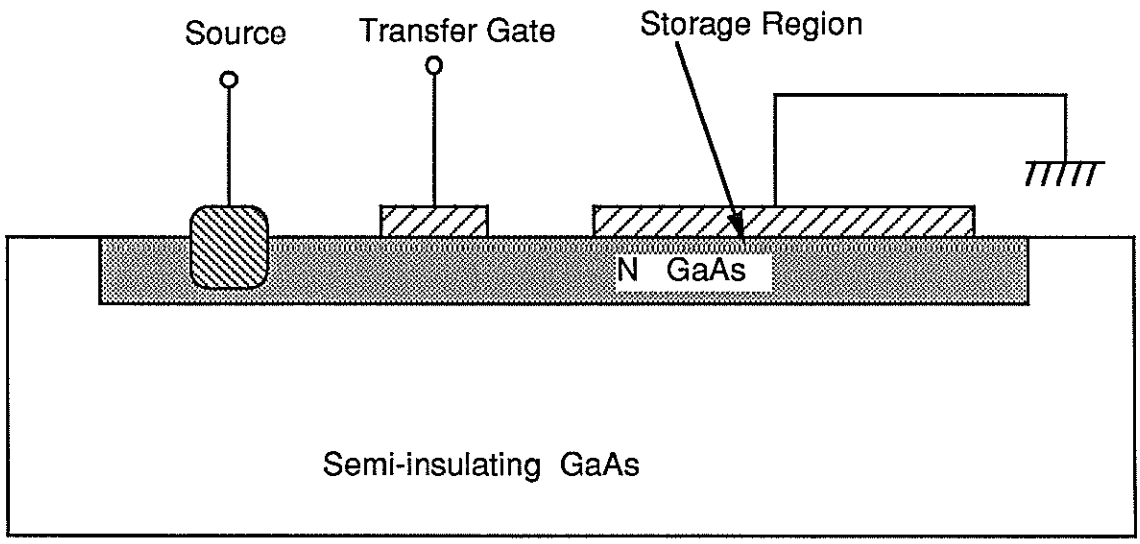

Figure 6. MESFET-isolated DRAM cell with Schottky barrier capacitor. The metal layer overlying the storage region forms a Schottky barrier with the N-layer underneath. Information is stored by reverse biasing this Schottky junction. This structure is fully compatible with existing MESFET fabrication processes, and would require NO additional fabrication steps.

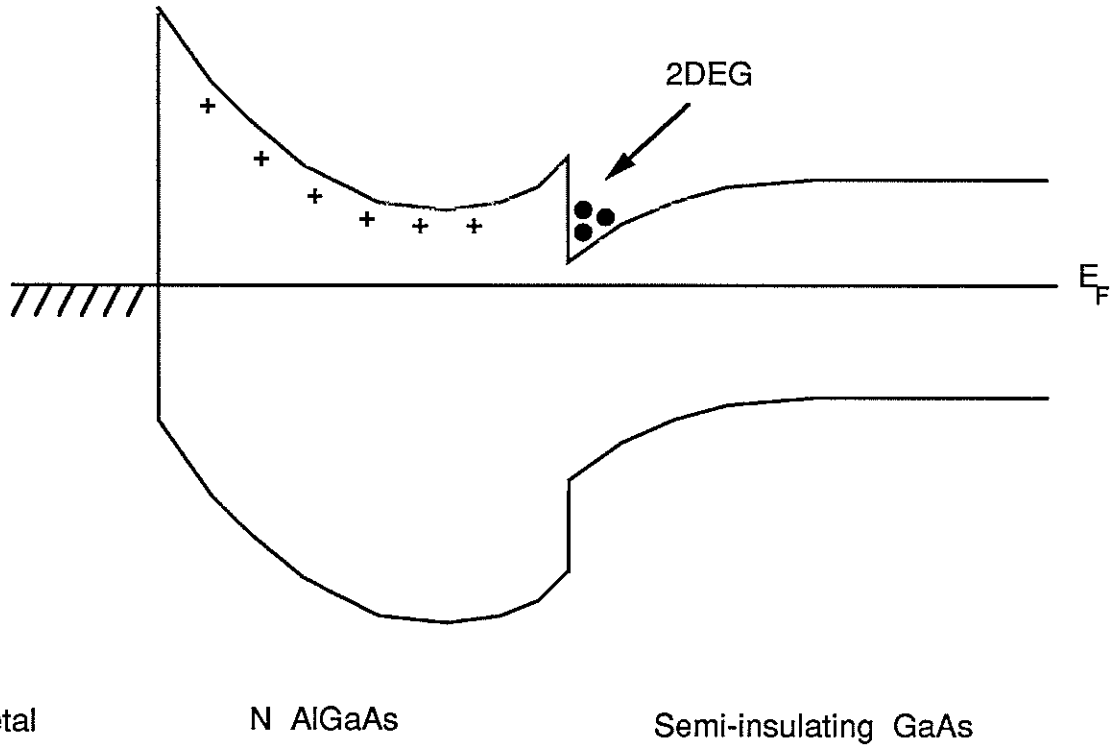

Figure 7. Band diagram for an AlGaAs/GaAs modulation-doped structure perpendicular to the surface. In this type of cell, a two-dimensional electron gas (2DEG) exists at the interface in equilibrium. Information is stored by selectively removing these electrons.

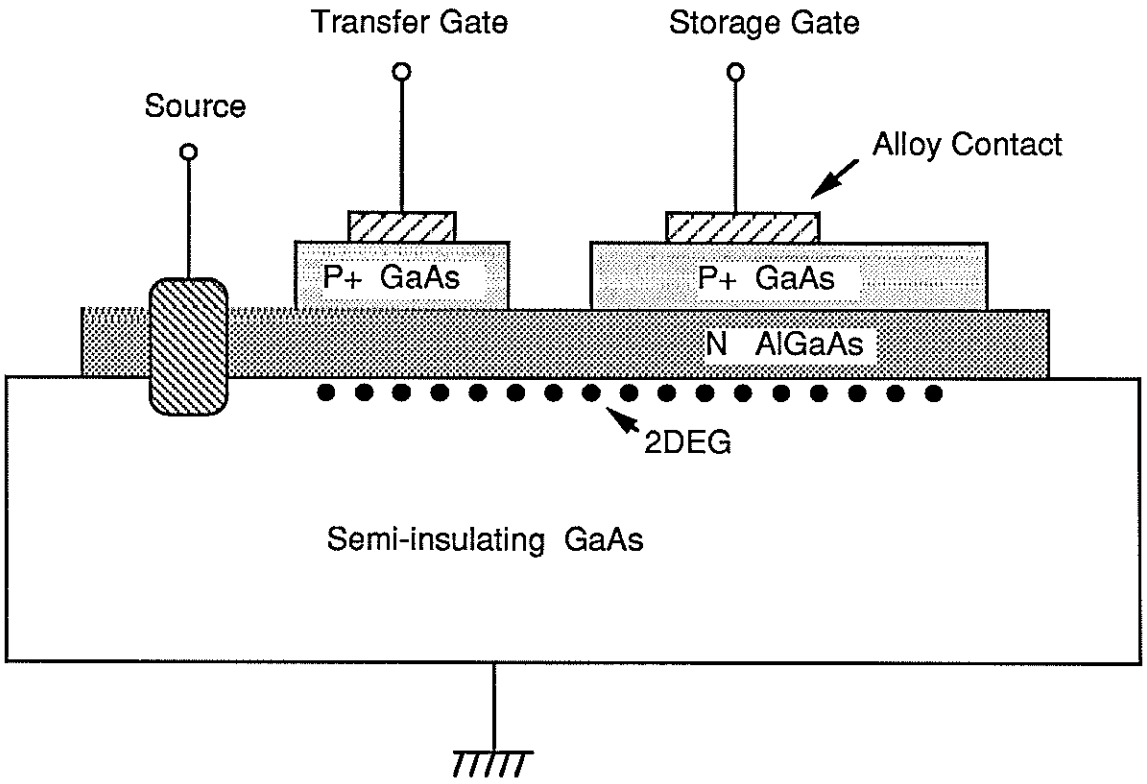

Figure 8. MODFET-isolated DRAM cell. This cell stores electrons at the interface between doped AlGaAs and undoped GaAs. This is a generation-imited memory, since the equilibrium condition is for a full 2DEG of electrons to exist at the interface. Information is stored by removing these electrons (in effect, by reverse biasing the gate-to-channel junction). Data is gradually lost by thermal generation, similar to the MESFET/JFET cells.

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8/88

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Activity: Student Member
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1978 to 1981
Member
1976 to 1978
1981 to Present

Organization: American Institute of Physics
Activity: Member
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Serial Journal Publications

[1] M.R. Melloch, R.L. Gunshor, C.L. Liu, and R.F. Pierret, "Interface Transduction in the ZnO—SiO_2—Si Surface Acoustic Wave Device Configuration," *Appl. Phys. Lett.,* Vol. 37(2), July 1980.

[2] M.R. Melloch, R.L. Gunshor, and R.F. Pierret, "Sezawa to Rayleigh Mode Conversion in the ZnO—on—Si Surface Acoustic Wave Device Configuration," *Appl. Phys. Lett.,* Vol. 39(6), September 1981.

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Lett. 52, 2255 (1988).

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[35] H. L. Chuang, P. D. DeMoulin, M. E. Klausmeier-Brown, M. R. Melloch, and M. S. Lundstrom, "Evidence for Bandgap Narrowing Effects in Be-doped, $p-p^+$ GaAs homojunction Barriers," J. Appl. Phys. 64, (1988).

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[1] M.R. Melloch, R.L. Gunshor, and R.F. Pierret, "Conversion of Sezawa to Rayleigh Waves in the $ZnO-SiO_2-Si$ Configuration," 1981 Ultrasonics Symposium Proceedings, Chicago, IL.

[2] R.D. Cherne, M.R. Melloch, R.L. Gunshor, and R.F. Pierret, "Bias Stable ZnO-on-Si SAW Devices," 1981 Ultrasonics Symposium Proceedings, Chicago, IL.

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[10] M.R. Melloch, S. Datta, S. Bandyopadhyay, R. Noren, M.S. Lundstrom, K. Tan, T. Dungan, R. Reifenberger, and M. Vaziri, "Aharanov-Bohm Effect in an MBE Grown Double Quantum Well," Sixth Molecular Beam Epitaxy Workshop, Minneapolis, MN (14-16 August 1985).

[11] S. Bandyopadhyay, M. Cahay, S. Datta, and M.R. Melloch, "Electron Transport in Ultrasmall Devices - Quantum Mechanical Effects," The Second International Conference (Yamada Conference) on Modulated Semiconductor Structures, Kyoto, Japan (9-13 September 1985).

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[20] M. R. Melloch, J. A. Cooper, Jr., and Q-D. Qian, "Investigation of Minority Carrier Hole Retention Behind AlAs and AlAs/GaAs Superlattice Barriers," Seventh US MBE Workshop, Boston, MA, October 20-22, 1986.

[21] S. Bandyopadhyay, M. R. Melloch, S. Datta, B. Das, J. A. Cooper, Jr., and M. S. Lundstrom, "A Novel Quantum Interference Transistor (QUIT) with Extremely Low Power-Delay Product and Very High Transconductance," 1986 International Electron Devices Meeting Technical Digest, Los Angeles, CA.

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[24] M. Vaziri, R. L. Gunshor, L. A. Kolodziejski, and M. R. Melloch, "Characterization of ZnSe on GaAs Epilayers," March Meeting of the American Physical Society, New York, New York, March 16-20, 1987.

[25] L. A. Kolodziejski, R. L. Gunshor, M. Melloch, M. Vaziri, C. Choi, and N. Otsuka, "MBE of ZnSe on GaAs Epilayers," SPIE's conference on Growth of Compound Semiconductors, Bay Point, Florida, March 26-27, 1987.

[26] P. D. DeMoulin, C. S. Kyono, M. S. Lundstrom, and M. R. Melloch, "Dark IV Characterization of GaAs p/n Heteroface Cells," 19th Photovoltaic Specialist Conference, New Orleans, Louisiana, May 4-8, 1987.

[27] M. E. Klausmeier-Brown, C. S. Kyono, D. P. Rancour, M. S. Carpenter, M. R. Melloch, M. S. Lundstrom, and R. F. Pierret, "Experimental Characterization of Minority Carrier Mirrors for GaAs-Based Solar Cells," 19th Photovoltaic Specialist Conference, New Orleans, Louisiana, May 4-8, 1987.

[28] G. S. Studtmann, R. L. Gunshor, L. A. Kolodziejski, M. R. Melloch, N. Otsuka, D. P. Munich, J. A. Cooper, and R. F. Pierret, "Pseudomorphic ZnSe/GaAs MISFET Devices," 45th Device Research Conference, University of California at Santa Barbara, June 22-24, 1987.

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[32] R. L. Gunshor, L. A. Kolodziejski, M. R. Melloch, N. Otsuka, and A. V. Nurmikko, "II-VI/III-V Heterointerfaces: Epilayer-on-Epilayer Structures," NATO Advanced Research Workshop on Growth and Optical Properties of Wide Gap II-VI's Low Dimensional Semiconductors, Regensburg, F. R. Germany, August 2-5, 1988.

[33] Q-D. Qian, J. Qiu, G. D. Studtmann, R. L. Gunshor, L. A. Kolodziejski, M. R. Melloch, J. A. Cooper, Jr., and M. Kobayashi, "Passivation of Epitaxial GaAs with Epitaxial ZnSe," 5th International Molecular Beam Epitaxy Conference, Sapporo, Japan.

[34] M. E. Klausmeier-Brown, P. E. Dodd, M. S. Lundstrom, and M. R. Melloch, "Heteroface Bipolar Transistor Based on Bandgap Narrowing in p^+—GaAs," 1988 Bipolar Circuits and Technology Meeting, Minneapolis, MN, September 12-13, 1988.

[35] M. S. Carpenter, M. R. Melloch, and T. E. Dungan, "Formation of Schottky Barriers on Reduced Surface State GaAs," 1988 International Symposium on Gallium Arsenide and Related Compounds," Atlanta, Georgia, September 11-14, 1988.

[36] J. S. Kleine, Q-D Qian, J. A. Cooper, Jr., and M. R. Melloch, "Mathematical Model for Carrier Emission from a Static Two-Dimensional Electron Gas," 1988 International Symposium on Gallium Arsenide and Related Compounds," Atlanta, Georgia, September 11-14, 1988.

[37] M. E. Klausmeier-Brown, P. D. DeMoulin, M. S. Lundstrom, M. R. Melloch, and S. P. Tobin, "Influence of Bandgap Narrowing Effects in p^+—GaAs on Solar Cell Performance," Twentieth IEEE Photovoltaic Specialists Conference, Las Vegas, Nevada, September 26-30, 1988.

Technical Reports

[1] M.R. Melloch, R.L. Gunshor, R.F. Pierret, and R.D. Cherne, "Zinc Oxide on Silicon Surface Acoustic Wave Devices," TR-EE 82-6, School of Electrical Engineering, Purdue University, February 1982.

[2] R.S. Wagers and M.R. Melloch, "Development of SAW Monolithic Memory Correlators for Adaptive Coherent Receivers," Final Technical Report on Contract No. N00014-81-C-0566, March 5, 1984.

[3] Qi-De Qian, James A. Cooper, Jr., and M. R. Melloch, "Measurement of Minority Carrier Retention Time at $Al_xGa_{1-x}As$ Interface," TR-EE 86-16, School of Electrical Engineering, Purdue University, June 1986.

[4] M. S. Lundstrom, M. R. Melloch, C. S. Kyono, C. P. McMahon, R. E. Noren, and D. P. Rancour, "Basic Studies of III-V High Efficiency Cell Components," TR-EE 86-35, School of Electrical Engineering, Purdue University, 8/15/85 - 8/14/86.

[5] M. S. Lundstrom, M. R. Melloch, R. F. Pierret, P. D. DeMoulin, D. P. Rancour, C. S. Kyono, and M. S. Carpenter, "Basic Studies of III-V High Efficiency Cell Components," TR-EE 87-33, School of Electrical Engineering, Purdue University, September 1987.

[6] Philip G. Neudeck, M. R. Melloch, and James A. Cooper, Jr., "Experiments in Interrupted Growth Molecular Beam Epitaxy Technology," TR-EE 88-3, School of Electrical Engineering, Purdue University, January 1988.

Patents

"ZnO SAW Device Having Separate Comb Transducer," No. 4,437,031, March 13, 1984.
"Photochemical Patterning," No. 4,612,085, September 1986.
"Buried Well DRAM," pending

VITA
1/88

Name: James A. Cooper, Jr. SSN: (b) (6)

Personal:

Date of Birth: (b) (6)
Place of Birth:
Citizenship:
Marital Status:
Wife's Name:
Children's names and Birthdates:

Education

Degree	*Date*	*School*
BSEE	1968	Mississippi State University
MSEE	1969	Stanford University
Ph.D.	1973	Purdue University

Thesis:

"A Unified Treatment of the Conductance, Capacitance, and Noise Due to Surface States at the SiO_2 Si Interface"

Professional Experience:

1968 — 1970	Member Technical Staff, Sandia Laboratories, Albuquerque, N.M.
	Principal activity: Evaluated radiation tolerance of MOS integrated circuits and developed circuit techniques to enhance radiation tolerance.
1973 — 1983	Member Technical Staff, Bell Laboratories, Murray Hill, N.J.
	Principal activities:
1973	Designed CCD serial memory access circuitry.
1974	Designed BTL's first CMOS IC, a 256-bit RAM.
1975	Designed BTL's largest and most complex IC to date, a 500-gate control chip for bubble repertory dialer telephone set.
1976 — 1977	Served as principal designer for the Bellmac-8 microprocessor, BTL's first microprocessor.
1978	Evaluated the performance and ultimate limitations of several competing VLSI technologies for long range planning purposes.

Dec. 1978	Transferred from the Electronic Component Development Area to the Research Area.
1979	Developed a polysilicon source and drain IGFET technology. Developed (with D. Kahng) a buried-drain DMOS technology.
1980 — 1983	Developed (with D.F. Nelson) a technique for obtaining a direct measurement of the drift velocity of carriers along semiconductor interfaces, the "interface time-of-flight" technique. Obtained detailed velocity-field data for electrons and holes at the SiO_2 — Si interface at high tangential fields.

Professional Society Activities

Organization:	IEEE
Activity:	Student member 1966 - 1969 Member 1969 - 1971 Student Member 1971 - 1973 Member 1973 - 1985 Senior Member 1985 - present
Activity:	Session Chairman 1982 IEEE Semiconductor Interface Specialists Conference, San Diego, CA Dec. 1982
Activity:	Associate Editor for Solid State, IEEE TRANSACTIONS ON ELECTRON DEVICES March 1983 - March 1986
Activity:	Member of Program Committee and Session Chairman, 1987 IEEE International Electron Devices Meeting, Washington, DC, Dec. 1987.

Research Book Contributions and Books Published:

[1] D. F. Nelson and J. A. Cooper, Jr., "High Field Surface Drift Velocities in Silicon," in *The Physics of Submicron Structures,* H. L. Grubin, K. Hess, G. J. Iafrate, and D. K. Ferry, eds., Plenum Publishing Co., 1984.

[2] J. A. Cooper, Jr., D. F. Nelson, S. A. Schwartz, and K. K. Thornber, "Effects on Carrier Velocity at Interfaces," book chapter in *VLSI Electronics: Microstructure Science,* N. G. Einspruch and R. S. Bauer, eds., Vol. 10, pp. 323-361, Academic Press, 1985.

Serial Journal Regular Articles:

[1] J. A. Cooper, Jr., E. R. Ward, and R. J. Schwartz, "Surface States and Insulator Traps at the Si_3N_4 – GaAs Interface," *Solid State Electronics,* Vol. 15, pp. 1219-1227, Nov. 1972.

[2] J. A. Cooper, Jr. and R. J. Schwartz, "Electrical Characteristics of the SiO_2 – Si Interface Near Midgap and in Weak Inversion," *Solid State Electronics,* Vol. 17, pp. 641-654, July 1974.

[3] J. A. Cooper, Jr., "Limitations on the Performance of Field-Effect Devices for Logic Applications," (Invited Paper), *Proceedings of the IEEE,* Vol. 69, pp. 226-231, Feb. 1981.

[4] D. F. Nelson and J. A. Cooper, Jr., "High-Field Electron Velocities in Silicon Surface Inversion Layers," *Surface Science,* Vol. 113, pp. 267-272, 1982.

[5] W. Fichtner, J. A. Cooper, Jr., A. R. Tretola, and D. Kahng, "A Novel Buried-Drain DMOSFET Structure," *IEEE Transactions on Electron Devices,* Vol. ED-29, pp. 1785, 1791, Nov. 1982.

[6] J. A. Cooper, Jr., and D. F. Nelson, "High-Field Drift Velocity of Electrons at the SiO_2 – Si Interface as Determined by a Time-of-Flight Technique," *J. Applied Physics,* Vol. 54, pp. 1445-1456, March 1983.

Serial Journal Correspondence or Letters:

[1] J. A. Cooper, Jr., "The Effect of an Energy-Dependent Capture Cross Section on Data Interpretation Using the MOS Conductance Technique," *J. Applied Physics,* Vol. 44, pp. 5613-5614, Dec. 1973.

[2] J. A. Cooper, Jr. and D. F. Nelson, "Measurement of the High-Field Drift Velocity of Electrons in Inversion Layers on Silicon," *IEEE Electron Device Letters,* Vol. EDL-2, pp. 171, 173, July 1981.

[3] K. K. Thornber, D. F. Nelson, and J. A. Cooper, Jr., "Cube-Root Broadening of Surface Charge Packets," *Applied Physics Letters,* Vol. 39, pp. 843-845, Nov. 15, 1981.

[4] A. K. Sinha, J. A. Cooper, Jr., and H. J. Levinstein, "Speed Limitations Due to Interconnect Time Constants in VLSI Integrated Circuits," *IEEE Electron Device Letters,* Vol. EDL-3, pp. 90-92, April 1982.

[5] D. F. Nelson, J. A. Cooper, Jr., and A. R. Tretola, "High-Field Drift Velocity of Holes in Inversion Layers on Silicon," *Applied Physics Letters,* Vol. 41, pp. 857-859, Nov. 1, 1982.

[6] J. A. Cooper, Jr., F. Capasso, and K. K. Thornber, "Semiconductor Structures for Repeated Velocity Overshoot," *IEEE Electron Device Letters,* Vol. EDL-3, pp. 407-408, Dec. 1982.

[7] D. F. Nelson, D. L. Abraham, and J. A. Cooper, Jr., "Measurement of Cube-Root Broadening of Charge Packets in MOS Structures," *Applied Physics Letters,* Vol. 42, pp. 815-817, May 1, 1983.

[8] J. A. Cooper, Jr., "Power Law Broadening of Charge Packets at Semiconductor Interfaces," *Applied Physics Letters,* Vol 44, pp. 243-245, Jan. 15, 1984.

[9] J. A. Cooper, Jr. and K. K. Thornber, "Screened-Charge Transferred-Electron Oscillators," *IEEE Electron Device Letters,* Vol. EDL-6, pp. 50-53, Jan. 1985.

[10] J. A. Cooper, Jr., Q-D. Qian, and M. R. Melloch, "Capacitance Voltage and Current Voltage Characteristics of Molecular Beam Epitaxially Grown P^+-GaAs/AlAs/N-GaAs Heterostructures," *Applied Physics Letters,* Vol. 48, pp. 365-366, Feb. 3, 1986.

[11] Q-D. Qian, M. R. Melloch, and J. A. Cooper, Jr., "Photosensitive Capacitance Voltage Characteristics of Molecular Beam Epitaxially Grown GaAs/AlGaAs/GaAs Heterostructures," *Applied Physics Letters,* Vol. 48, pp. 638-640, March 10, 1986.

[12] J. A. Cooper, Jr., Q-D. Qian, and M. R. Melloch, "Evidence of Long-Term Storage of Minority Carriers in N^+-GaAs/AlGaAs/P-GaAs MIS Capacitors," *IEEE Electron Device Letters,* Vol. EDL-7, June 1986.

[13] Q-D. Qian, M. R. Melloch, J. A. Cooper, Jr., "Multi-Day Storage of Holes at the AlAs/GaAs Interface," *IEEE Electron Dev. Lett.,* EDL-7, 607 (1986).

[14] M. R. Melloch, Q-D. Qian, and J. A. Cooper, Jr., "Long Term Storage of Inversion Holes at a Superlattice/GaAs Interface," *Appl. Phys. Lett.,* 49, 1471 (1986).

[15] M. R. Melloch, C. P. McMahon, M. S. Lundstrom, J. A. Cooper, Jr., Q-D. Qian, and S. Bandyopadhyay, "Bias-Dependent Photoresponse of p+in GaAs/AlAs/GaAs Diodes," *Appl. Phys. Lett.,* Vol. 50, pp. 161-163, Jan. 19, 1987.

[16] M. R. Melloch, J. A. Cooper, Jr., and Q-D. Qian, "Investigation of Minority Carrier hole Retination Behind AlAs and AlAs/GaAs Superlattice Barriers," *J. Vac. Sci. and Tech.,* Vol. B5, pp. 766-769, May-June 1987.

[17] M. R. Melloch, C. P. McMahon, M. S. Lundstrom, J. A. Cooper, Jr., and Q-D. Qian, "Photocollection Efficiency of GaAs/AlAs/GaAs p+ and n+ Photodiodes," *Solar Cells,* Vol. 21, pp. 233-240, 1987.

[18] T. E. Dungan, J. A. Cooper, Jr., and M. R. Melloch, "A Thermal-Generation-Limited Buried-Well Structure for Room-Temperature GaAs Dynamic RAM's," *IEEE Electron Dev. Lett.,* Vol. EDL-8, pp. 243-245, May 1987.

[19] M. R. Melloch, Q-D. Qian, and J. A. Cooper, Jr., "Effect of a Buried Superlattice on the Dynamic Storage of Electrons at the AlGaAs/GaAs Heterojunction," *Appl. Phys. Lett.,* Vol. 50, pp. 1657-1659, June 8, 1987.

Conference Proceedings and Presentations:

[1] J. A. Cooper, Jr., "Effects of Ionizing Radiation on Monolithic MOS Inverters," IEEE Nuclear and Space Radiation Effects Conference, San Diego, CA, 1970.

[2] J. A. Cooper, Jr., and R. J. Schwartz, "Electrical Characteristics of the $Si0_2$ — Si Interface Near Midgap and in Weak Inversion," IEEE Device Research Conference, Boulder, CO, June 26-28, 1973.

[3] J. A. Cooper, Jr., J. A. Copeland, R. H. Krambeck, D. C. Stanzione, and L. C. Thomas, "A CMOS Microprocessor for Telecommunications Applications," IEEE International Solid State Circuits Conf., Philadelphia, PA, Feb. 16-18, 1977.

[4] J. A. Cooper, Jr., and D. F. Nelson, "Observation of High-Field Transport in Silicon Inversion Layers by a Time-of-Flight Technique," IEEE Device Research Conference, Ithica, NY, June 23-25, 1980.

[5] J. A. Cooper, Jr. and D. F. Nelson, "High-Field Drift Velocity of Electrons in Silicon Inversion Layers as Determined by a Time-of-Flight Technique," IEEE Semiconductor Interface Specialists Conf., Ft. Lauderdale, FL, Dec. 4-6, 1980.

[6] D. F. Nelson and J. A. Cooper, Jr., "High-Field Electron Velocities in Silicon Surface Inversion Layers," American Physical Society Spring Meeting, Phoenix, AZ, March 16-20, 1981.

[7] D. F. Nelson and J. A. Cooper, Jr., "High-Field Electron Velocities in Silicon Surface Inversion Layers," Electronic Properties of Two-Dimensional Systems IV, New London, NH, Aug. 24-28, 1981.

[8] K. K. Thornber, D. F. Nelson, and J. A. Cooper, Jr., "Cube-Root Broadening of Space Charge Packets," IEEE Semiconductor Interface Specialists Conf., New Orleans, LA, Dec. 4-6, 1981.

[9] W. Fichtner, J. A. Cooper, Jr., A. R. Tretola, and D. Kahng, "A Novel Buried Drain DMOSFET Structure," IEEE International Electron Devices Meeting, Washington, DC, Dec. 7-9, 1981.

[10] J. A. Cooper, Jr., "Performance Limitations Due to On-Chip Interconnects in VLSI Integrated Circuits," (Invited Paper) *1982 IEEE VLSI Workshop,* Hyannis, MA, May 6-7, 1982.

[11] D. F. Nelson and J. A. Cooper, Jr., "High Field Surface Drift Velocities in Silicon," (Invited Paper) Physics of Sub-Micron Structures Conf., Urbana, IL, June 1982.

[12] D. F. Nelson, D. L. Abraham, and J. A. Cooper, Jr., "Measurement of Cube-Root Broadening of Charge Packets in MOS Structures," American Physical Society Spring Meeting, Los Angeles, CA, March 1983.

[13] J. A. Cooper, Jr. and K. K. Thornber, "Contiguous-Domain Transferred-Electron Oscillators," IEEE International Microwave Symposium, St. Louis, MO, June 4-6, 1985.

[14] J. A. Cooper, Jr. and K. K. Thornber, "A Contiguous-Domain Transferred-Electron Oscillator," *IEEE Device Research Conference,* Boulder, CO, June 17-19, 1985.

[15] J. A Cooper, Jr., "High Field Drift Velocity Measurement in Inversion Layers on Silicon," (Invited Paper) 1985 Conference on Solid-State Devices and Materials, Tokyo, JAPAN, August 25-27, 1985.

[16] M. R. Melloch, J. A. Cooper, Jr., and Q-D. Qian, "Photosensitive C-V Characteristics of MBE-Grown GaAs/AlGaAs/GaAs Heterostructures," 1985 Fall Meeting of the Midwest MBE Users Group, Wright State University, October 29, 1985.

[17] M. R. Melloch, J. A. Cooper, Jr., and Q-D. Qian, "Minority Carrier Retention at the GaAs/AlGaAs Interface," American Physical Society Topical Conf. on III-V and II-VI Compound Semiconductor Surfaces, Atlanta, GA, Jan. 27-28, 1986.

[18] M. R. Melloch, J. A. Cooper, Jr., and Q-D. Qian, "Investigation of Minority Carrier Hole Retention Behind AlAs and AlAs/GaAs Superlattice Barriers," Seventh US MBE Workshop, Boston, MA, October 20-22, 1986.

[19] J. A. Cooper, Jr., M. R. Melloch, and Q-D. Qian, "Development of a One Transistor Dynamic RAM for the AlGaAs/GaAs HIGFET Technology," *IEEE Intl. Electron Devices Meeting,* Los Angeles, CA, Tech. Digest, pp. 452-455, Dec. 1986. 452, 1986.

[20] J. A. Cooper, Jr., "The Contiguous-Domain Oscillator-Concept and Realization," WOCSEMMAD Conf., Hilton Head, SC, March 2-4, 1987.

[21] G. D. Studtmann, R. L. Gunshor, L. A. Kolodziejski, M. R. Melloch, N. Otsuka, D. P. Munich, J. A. Cooper, Jr., and R. F. Pierret, "Pseudomorphic ZnSe/GaAs MISFET

Devices," *IEEE Device Research Conf.,* Santa Barbara, CA, June 1987.

[22] T. E. Dungan, J. A. Cooper, Jr., and M. R. Melloch, "Room Temperature Dynamic Memories for GaAs Integrated Circuits," *IEEE International Electron Devices Meeting,* Washington, DC, Tech. Digest, pp. 348-351, Dec. 1987.

Invited Lectures:

[1] J. A. Cooper, Jr., "Dynamic Behavior of Electrons at Semiconductor Interfaces Under High-Field Conditions," Yale University, New Haven, CT, May 1984.

[2] J. A. Cooper, Jr., "Dynamic Memory Elements for the High-Electron-Mobility-Transistor (HEMT) Technology," Kodak Research Laboratories, Rochester, NY, Sept. 1984.

[3] J. A. Cooper, Jr., "One-Transistor Dynamic Memory Cells for GaAs Integrated Circuits," IBM T. J. Watson Research Center, Yorktown Heights, NY, Dec. 1984.

[4] J. A. Cooper, Jr., "Observation of High Field Transport in Silicon Inversion Layers," Nippon Telegraph and Telephone Corp. Atsugi Electrical Communication Laboratories, Atsugi-shi, JAPAN, August 19, 1985.

[5] J. A. Cooper, Jr., "Measurement of High Field Drift Velocity at Semiconductor Interfaces Using a Time-of-Flight Technique," Fujitsu Laboratories, Atsugi-shi, JAPAN, August 19, 1985.

[6] J. A. Cooper, Jr., "High-Field Electron Transport at the Silicon-Silicon Dioxide Interface," Toshiba Research and Development Center, Kawasaki, JAPAN, August 20, 1985.

[7] J. A. Cooper, Jr., "The High-Field Drift Velocity in Silicon Inversion Layers," Special Seminar, Kansai Branch of Japan Society of Applied Physics, Osaka, JAPAN, August 21, 1985.

[8] J. A. Cooper, Jr. and M. R. Melloch, "One-Transistor Dynamic Memory Cells for GaAs Integrated Circuits," AT&T Bell Laboratories, Murray Hill, NJ, Sept. 1987.

[9] J. A. Cooper, Jr. and M. R. Melloch, "Dynamic Storage of Majority and Minority Carriers in GaAs," Bell Communications Research, Inc., Red Bank, NJ, Sept. 1987.

Technical Reports:

[1] J. A. Cooper, Jr., "Effects of Ionizing Radiation on Monolithic MOS Inverters," SC-TM-70-339, Sandia Laboratories, June 1970.

[2] J. A. Cooper, Jr. and R. J. Schwartz, "A Unified Treatment of the Conductance, Capacitance, and Noise due to Surface States at the $Si0_2 - Si$ Interface," TR-EE-73-20, School of Electrical Engineering, Purdue University, August 1973.

[3] J. A. Cooper, Jr. and A. M. Mohsen, "Design Considerations and Performance Predictions for Two-Phase Offset Charge Coupled Devices with Particular Reference to Their Use in Mass Memory," TM-74-2251-11, Bell Laboratories, April 12, 1974.

[4] J. A. Cooper, Jr., "A Numerical Solution of the Two-Dimensional Poisson Equation for the Short-Channel IGFET with Non-Uniform Channel Doping," TM-78-2111-14, Bell Laboratories, Sept. 13, 1978.

[5] S. M. Kang and J. A. Cooper, Jr., "Design of 3.5 μm CMOS Polycells," TM 79-1151-1, Bell Laboratories, Jan. 8, 1979.

[6] J. A. Cooper, Jr., "Interconnect Capacitance in Integrated Circuits Under Design Rule Scaling," TM-79-1151-24, Aug. 27, 1979.

[7] J. A. Cooper, Jr., D. V. Speeney, and T. T. Sheng, "A Polysilicon Source and Drain Recessed-Channel IGFET," TM-81-11151-3, Bell Laboratories, Jan 26, 1981.

[8] J. A. Cooper, Jr. and M. G. Lamont, "Numerical Simulation of Surface Charge Transport in Silicon and GaAs," TM-83-11156-13, Bell Laboratories, July 18, 1983.

[9] J. A. Cooper, Jr., "Power Law Broadening of Charge Packets at Semiconductor Interfaces," TM 83 11156-14, Bell Laboratories, July 18, 1983.

(Several other Bell Laboratories Technical Memoranda are omitted here because they were subsequently published in the open literature and are listed elsewhere in this vita.)

[10] Q-D. Qian, J. A. Cooper, Jr., and M. R. Melloch, "Measurement of Minority Carrier Retention Time at $Al_xGa_{1-x}As$/GaAs Interface," TR-EE 86-16, School of Electrical Engineering, Purdue University, June 1986.

[11] J. S. Kleine and J. A. Cooper, Jr., "Rapid Thermal Annealing of Silicon Implanted Gallium Arsenide," TR-EE 86-43, School of Electrical Engineering, Purdue University, December 1986.

[12] P. G. Neudeck, M. R. Melloch, and J. A. Cooper, Jr., "Experiments in Interrupted Growth Molecular Beam Epitaxy Technology," TR-EE 88-3, School of Electrical Engineering, Purdue University, January 1988.

Patents:

[1] J. A. Cooper, Jr., "Apparatus and Method for Regenerating Charge," U.S. Patent #3,937,985, Feb. 10, 1976.

[2] D. E. Blahut and J. A. Cooper, Jr., "Integrated Read Only Memory," U.S. Patent #4,139,907, Feb. 13, 1979.

[3] D. E. Blahut and J. A. Cooper, Jr., "Programmable Logic Array," U.S. Patent #4,208,728, June 17, 1980.

[4] J. A. Cooper, Jr. and R. H. Krambeck, "Multistage Logic Circuit Arrangement," U.S. Patent #4,291,247, Sept. 1981.

[5] C. C. Chang, J. A. Cooper, Jr., D. Kahng, and S. P. Murarka, "Method of Fabricating MOS Field Effect Transistors," U.S. Patent #4,324,038, April 13, 1982.

[6] J. A. Cooper, Jr., "Memory Cell for HEMT," U.S. Patent #4,635,083, January 6, 1987.

[7] F. Capasso, J. A. Cooper, Jr., and K. K. Thornber, "Repeated Velocity Overshoot Semiconductor Device," U.S. Patent #4,719,496, January 12, 1988.

[8] J. A. Cooper, Jr. and K. K. Thornber, "Transferred Electron Device," U.S. Patent pending.

[9] J. A. Cooper, Jr., M. R. Melloch, and T. E. Dungan, "Buried Well Dynamic Memory Cell," U.S. Patent applied for.

(J. A. Cooper, Jr.)

Pending Publications:

[1] G. D. Studtmann, R. L. Gunshor, L. A. Kolodziejski, M. R. Melloch, N. Otsuka, D. P. Munich, J. A. Cooper, Jr., and R. F. Pierret, "A Pseudomorphic ZnSe/GaAs Doped Channel Field Effect Transistor," accepted by *Appl. Phys. Lett.*

CONTRACT PRICING PROPOSAL COVER SHEET

32

OMB NO. 3090-0116

NOTE: This form is used in contract actions if submission of cost or pricing data is required. (See FAR 15.804-6(b))

1. NAME AND ADDRESS OF OFFEROR (Include ZIP Code)	1A. NAME AND TITLE OF OFFEROR'S POINT OF CONTACT	1B. TELEPHONE NO.
Purdue Research Foundation Hovde Hall West Lafayette, IN For Technical Information contact: P.I.: Michael Melloch Phone: (317)494-3528	Thomas Wright	(317)494-1078

4. TYPE OF CONTRACT ACTION (Check)

X	A. NEW CONTRACT		D. LETTER CONTRACT
	B. CHANGE ORDER		E. UNPRICED ORDER
	C. PRICE REVISION/ REDETERMINATION		F. OTHER (Specify)

5. TYPE OF CONTRACT (Check)

☐ FFP ☐ FPI ☐ CPFF ☒ OTHER (Specify) Cost-Reimbursement ☐ CPIF ☐ CPAF

6. PROPOSED COST (A+B=C)

A. COST	B. PROFIT/FEE	C. TOTAL
$ 305,000	$ 0	$ 305,000

7. PLACE(S) AND PERIOD(S) OF PERFORMANCE

Purdue University
School of Electrical Engineering. Period of Performance: 06/01/89 - 12/31/91

List and reference the identification, quantity and total price proposed for each contract line item. A line item cost breakdown supporting this recap is required unless otherwise specified by the Contracting Officer. (Continue on reverse, and then on plain paper, if necessary. Use same headings.)

A. LINE ITEM NO.	B. IDENTIFICATION	C. QUANTITY	D. TOTAL PRICE	E. REF.
I	Salaries & wages		$147,281	
II.	Grad Fee Remission		8,100	
III.	Fringe Benefits		(b) (4)	
IV.	Travel Domestic		5,150	
V.	Expendable Equipment		6,700	
VI.	Publication & Duplication		2,750	
VII.	Other: Communications-$230; Supplies-$15,500		15,730	
	Total direct cost		$211,457	
	Indirect cost (b) (4) of MTD cost		(b) (4)	
	Total cost		$305,000	

9. PROVIDE NAME, ADDRESS, AND TELEPHONE NUMBER FOR THE FOLLOWING (If available)

9A. CONTRACT ADMINISTRATION OFFICE
Office of Contract & Grant Business Affairs
Hovde Hall
Purdue University
West Lafayette, IN 47907 (317)494-1078

9B. AUDIT OFFICE
DHHS Audit Agency
Room 680
575 N. Pennsylvania Avenue
Indianapolis, IN 46204 (317)269-7837

10. WILL YOU REQUIRE THE USE OF ANY GOVERNMENT PROPERTY IN THE PERFORMANCE OF THIS WORK? (If "Yes," identify)
☐ YES ☒ NO

11A. DO YOU REQUIRE GOVERNMENT CONTRACT FINANCING TO PERFORM THIS PROPOSED CONTRACT? (If "Yes," complete item 11B)
☒ YES ☐ NO

11B. TYPE OF FINANCING (If any)
☒ ADVANCE PAYMENTS ☐ PROGRESS PAYMENTS
☐ GUARANTEED LOANS

12. HAVE YOU BEEN AWARDED ANY CONTRACTS OR SUBCONTRACTS FOR THE SAME OR SIMILAR ITEMS WITHIN THE PAST 3 YEARS? (If "Yes," identify item(s), customer(s) and contract number(s))
☐ YES ☒ NO

13. IS THIS PROPOSAL CONSISTENT WITH YOUR ESTABLISHED ESTIMATING AND ACCOUNTING PRACTICES AND PROCEDURES AND FAR PART 31 COST PRINCIPLES? (If "No," explain)
☒ YES ☐ NO

14. COST ACCOUNTING STANDARDS BOARD (CASB) DATA (Public Law 91-379 as amended and FAR PART 30)

14A. WILL THIS CONTRACT ACTION BE SUBJECT TO CASB REGULATIONS? (If "No," explain in proposal)
☐ YES ☒ NO Exempt under OMB circular A-21

14B. HAVE YOU SUBMITTED A CASB DISCLOSURE STATEMENT (CASB DS-1 or 21)? (If "Yes," specify in proposal the office to which submitted and if determined to be adequate)
☐ YES ☐ NO

14C. HAVE YOU BEEN NOTIFIED THAT YOU ARE OR MAY BE IN NONCOMPLIANCE WITH YOUR DISCLOSURE STATEMENT OR COST ACCOUNTING STANDARDS? (If "Yes," explain in proposal)
☐ YES ☐ NO

14D. IS ANY ASPECT OF THIS PROPOSAL INCONSISTENT WITH YOUR DISCLOSED PRACTICES OR APPLICABLE COST ACCOUNTING STANDARDS? (If "Yes," explain in proposal)
☐ YES ☐ NO

This proposal is submitted in response to the RFP contract, modification, etc. in Item 1 and reflects our best estimates and/or actual costs as of this date

15. NAME AND TITLE (Type)	16. NAME OF FIRM
Louis Pellegrino, Assistant Director Division of Sponsored Programs	Purdue Research Foundation

17. SIGNATURE	18. DATE OF SUBMISSION
(b) (6)	10/25/88

OFFICE NAVAL RESEARCH

For the period 06/01/89 through 05/31/90

A.	Salaries and Wages		
	1. Senior personnel		
	Principal Investigator		
	Michael Melloch	0.10 AY	(b) (4)
		**** SS	
	Principal Investigator		
	James Cooper	0.10 AY	
		**** SS	
	Subtotal		27420
	2. Other personnel		
	Graduate assistant		
	2 Grad Students	1.00 AY	16000
		2.00 SS	6400
	Total salaries & wages		49820
	Grad fee remission		3240
	Total compensation		53060
B.	Fringe Benefits		
	Total fringe benefits		(b) (4)
C.	Total compensation and fringes		60894
D.	Non-personnel direct costs		
	Communications		100
	Travel - Domestic		2000
	Publication & Duplication		1100
	Expendable equipment		2500
	Other S & E		6000
	Total non-personnel direct costs		11700
E.	Total direct cost		72594
F.	Indirect cost (b) (4) of MTD cost		(b) (4)
G.	Total cost	$	104497

OFFICE NAVAL RESEARCH

For the period 06/01/90 through 05/31/91

A.	Salaries and Wages		
	1. Senior personnel		
	Principal Investigator		
	Michael Melloch	0.15 AY	(b) (4)
		**** SS	
	Principal Investigator		
	James Cooper	0.15 AY	
		**** SS	
	Subtotal		36469
	2. Other personnel		
	Graduate assistant		
	2 Grad Students	1.00 AY	16000
		2.00 SS	6400
	Total salaries & wages		58869
	Grad fee remission		3240
	Total compensation		62109
B.	Fringe Benefits		
	Total fringe benefits		(b) (4)
C.	Total compensation and fringes		72395
D.	Non-personnel direct costs		
	Communications		100
	Travel - Domestic		2050
	Publication & Duplication		1100
	Expendable equipment		2500
	Other S & E		6000
	Total non-personnel direct costs		11750
E.	Total direct cost		84145
F.	Indirect cost (b) (4) of MTD cost		(b) (4)
G.	Total cost	$	121361

OFFICE NAVAL RESEARCH

For the period 06/01/91 through 12/31/91

A.	Salaries and Wages		
	1. Senior personnel		
	Principal Investigator		
	Michael Melloch	**** AY	(b) (4)
		**** SS	
	Principal Investigator		
	James Cooper	**** AY	
		**** SS	
	Subtotal		27392
	2. Other personnel		
	Graduate assistant		
	2 Grad Students	**** AY	8000
		**** SS	3200
	Total salaries & wages		38592
	Grad fee remission		1620
	Total compensation		40212
B.	Fringe Benefits		
	Total fringe benefits		(b) (4)
C.	Total compensation and fringes		47838
D.	Non-personnel direct costs		
	Communications		30
	Travel - Domestic		1100
	Publication & Duplication		550
	Expendable equipment		1700
	Other S & E		3500
	Total non-personnel direct costs		6880
E.	Total direct cost		54718
F.	Indirect cost (b) (4) of MTD cost		(b) (4)
G.	Total cost	$	79142

OFFICE NAVAL RESEARCH

For the period 06/01/89 through 12/31/91

A.	Salaries and Wages		
	1. Senior personnel		
	Principal Investigator		
	Michael Melloch	AY	(b) (4)
		SS	
	Principal Investigator		
	James Cooper	AY	
		SS	
	Subtotal		91281
	2. Other personnel		
	Graduate assistant		
	2 Grad Students	AY	40000
		SS	16000
	Total salaries & wages		147281
	Grad fee remission		8100
	Total compensation		155381
B.	Fringe Benefits		
	Total fringe benefits		(b) (4)
C.	Total compensation and fringes		181127
D.	Non-personnel direct costs		
	Communications		730
	Travel - Domestic		5150
	Publication & Duplication		2750
	Expendable equipment		6700
	Other S & E		15500
	Total non-personnel direct costs		30330
E.	Total direct cost		211457
F.	Indirect cost (b) (4) of MTD cost		(b) (4)
G.	Total cost	$	305000

PROPERTY LISTING

Government Furnished Property (be specific):

Description	Estimated Value
no items	

Property to be acquired with contract funds:
A. Items costing less than $5000.

Description	Estimated Value
no items	

B. Items costing $5000 or more.

Description	Estimated Value
no items	

In accordance with the Equipment Acquisition Statement submitted on March 26, 1984, Purdue Research Foundation hereby expresses its unwillingness or financial inability to acquire the above property within its existing resources.

Current and Pending Support for Research and Education in Science and Engineering

The following information should be provided for each investigator and other senior personnel. Failure to provide this information may delay consideration of the proposal.

I. Name of Principal Investigator: Michael R. Melloch	Source of Support	Project Title	Award Amount (or Annual Rate)	Period Covered by Award	Person-Months or % of Effort Committed to the Project			Location of Research
					ACAD.	SUMM.	CAL. YR.	
A. *Current Support* List—If none, report none	ONR	1)	$227,928	1)	2	1		Purdue University
	SERI	2)	$206,183	2)	2.5	1		Purdue University
	ICST	3)	$746,949	3)	1.5	1		Purdue University
	ONR	4)	$ 64,847	4)	0	0		Purdue University
	NSF	5)	$ 46,570	5)	0	0		Purdue University
B. *Proposals Pending* 1 List this proposal	ONR	6)	$461,643	6)	1	1		Purdue University
	NSF	7)	$240,474	7)	0	1		Purdue University
	ONR	8)	$305,001	8)	1	1		Purdue University
2. Other pending proposals, including renewal applications. If none, report none.								
3. Proposals planned to be submitted in near future. If none, report none.								
II. Name of co-principal investigator and/or faculty associate A. _____ B. _____								
III. Transfer of Support If this project has previously been funded by another agency, please list and furnish information for immediately preceding funding period.								
IV. Other agencies to which this proposal has been/will be submitted								

USE ADDITIONAL SHEETS AS NECESSARY

1) GaAs Gate Dynamic Memory Technology, 6/86-5/88
2) Basic Studies of High-Efficiency III-V Cell Components, 9/1/88-8/31/89
3) High Speed III-V Semiconductor Devices, 7/86-6/89
4) Quantum Interference Devices, 7/87-12/88
5) Engineering Research Equipment Grant: Mask Aligner, 9/88-9/89
6) Development of a GaAs Dynamic Content Addressable Memory, 7/88-2/91
7) Minority Carrier Transport in Heavily Doped GaAs, 1/1/89-12/31/91.
8) GaAs Gate Dynamic Memory Technology 06/01/89-12/31/91.

Current and Pending Support for Research and Education in Science and Engineering

The following information should be provided for each investigator and other senior personnel. Failure to provide this information may delay consideration of the proposal.

I. Name of Principal Investigator James A. Cooper, Jr.	Source of Support	Project Title	Award Amount (or Annual Rate)	Period Covered by Award	Person-Months or % of Effort Committed to the Project			Location of Research
					ACAD.	SUMM.	CAL. YR.	
A. *Current Support* List—if none, report none	ONR	1.	$227,928	1	1	1		Purdue University
	ECST	2.	746,949	2	1.5	1		Purdue University
	ONR/SDIO	3.	461,643	3	1	1		Purdue University
B. *Proposals Pending* 1. List this proposal	AFOSR	4.	16,823	4	0	0		Purdue University
	ONR	5.	305,001	5	1	1		Purdue University
2. Other pending proposals, including renewal applications. If none, report none.								
3. Proposals planned to be submitted in near future. If none, report none.								
II. Name of co-principal investigator and/or faculty associate A. _____ B. _____								
III. Transfer of Support If this project has previously been funded by another agency, please list and furnish information for immediately preceding funding period.								
IV. Other agencies to which this proposal has been/will be submitted								

USE ADDITIONAL SHEETS AS NECESSARY

1. GaAs Gate Dynamic Memory Technology 6/86-5/88
2. High Speed III-V Semiconductor Devices 7/86-6/89
3. Development of a GaAs Dynamic Content Addressable Memory 7/88-2/91
4. Continuation of Research on the Contiguous Domain Oscillator 1/89-4/90
5. GaAs Gate Dynamic Memory Technology 6/89-12/91